

Riot board

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Design	<design>	Embest Tech Co. LTD		
Review	<review>	Title:MX6		
Authorize	<authorize>	Size	Doc Name	Ver.
Standardize	<standardize>	A3	01.CONVER PAGE	V1.0
		Date	Saturday, December 07, 2013	Sheet 1 of 20

Schematic History

2013-07-19

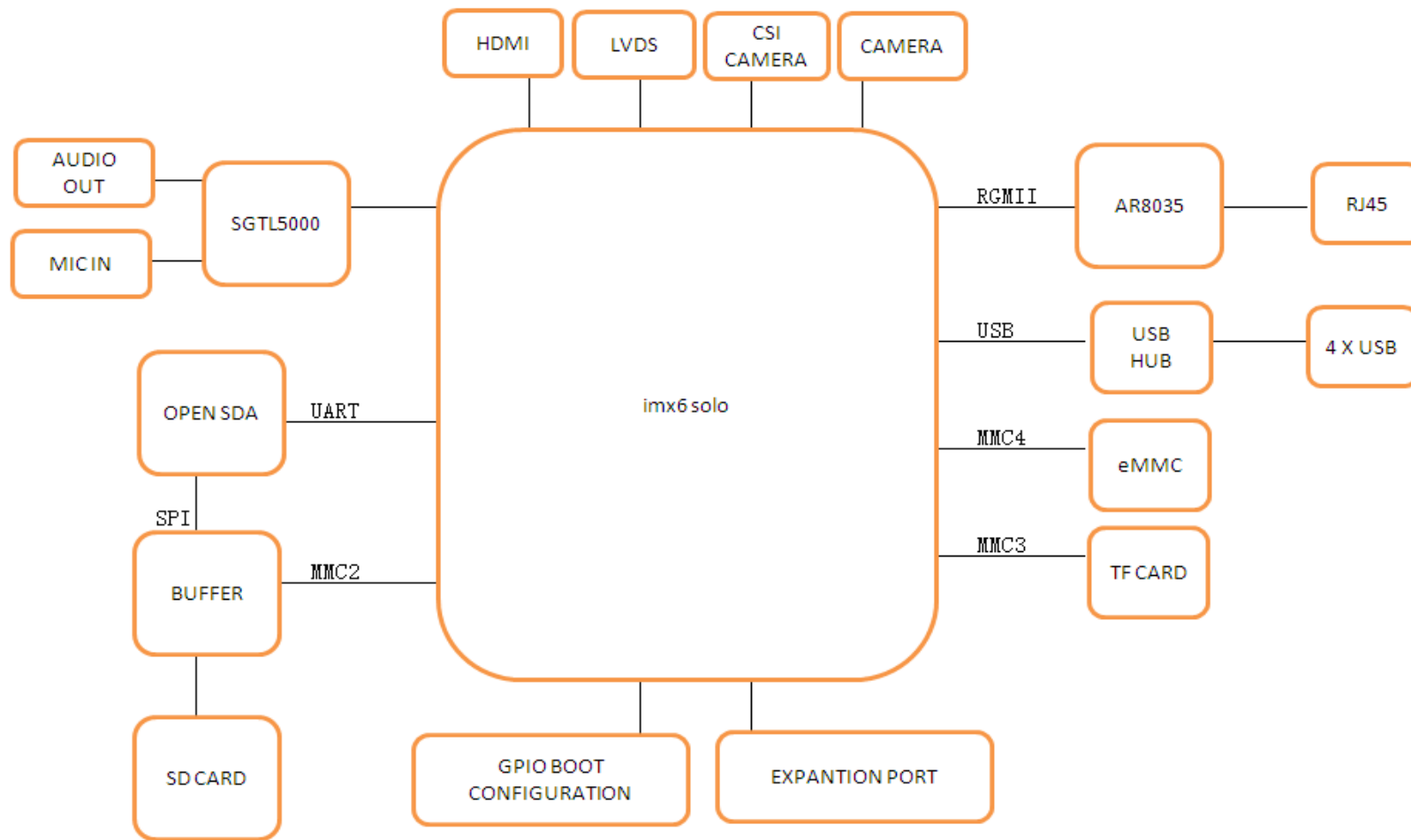
- 1.update all the parts reference to fix drc error
- 2.change bus SDA_SD4_* to SDA_SD2_* on PAGE(15)
- 3.add I2C2_SCL/SDA connect to PMIC (PAGE05)
- 4.remove TPS3808G33DBVT (PAGE18), use PMIC internal reset for IMX6(PAGE05)

2013-08-01

- 1.Separate RJ45+Dual USB

Design	<design>	Embest Tech Co. LTD		
Review	<review>	Title:MX6		
Authorize	<authorize>	Size	Doc Name	Ver.
Standardize	<standardize>	A3	02.Schematic History	V1.0
		Date	Saturday, December 07, 2013	Sheet 2 of 20

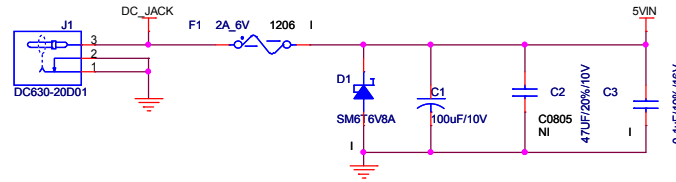
SYSTEM BLOCK



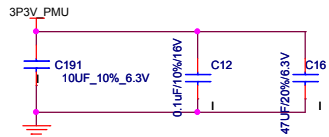
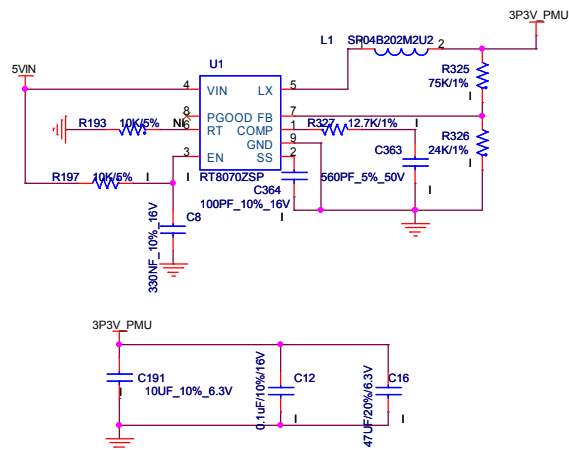
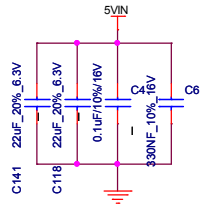
PCB1 PCB
1001001000234

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		Date	Saturday, December 07, 2013	Sheet 3 of 20

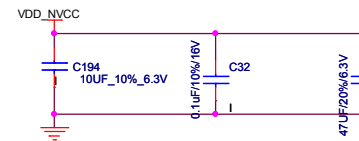
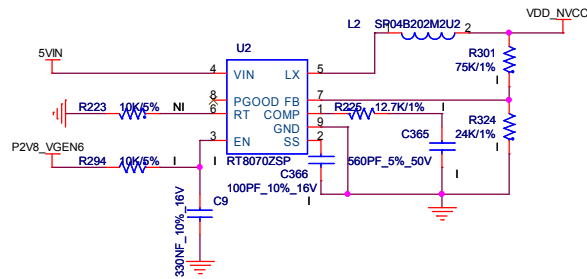
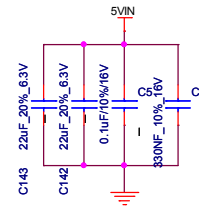
Main Power



PMIC Power Feed 3.5 A max



Peripheral Power Supply 3.5 A max

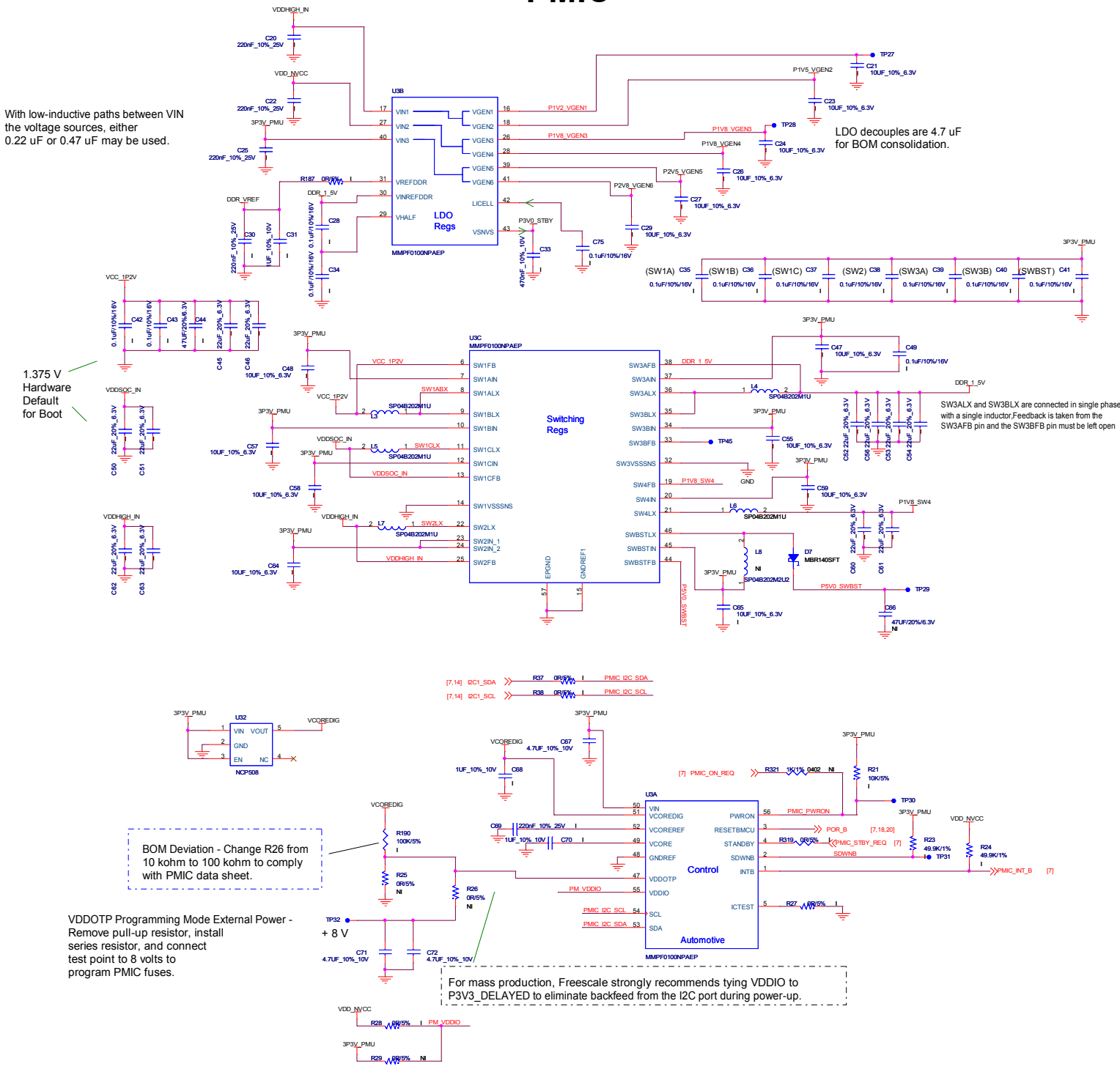


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Standardize	<standardize>	A3	04 MAIN POWER	V1.0
		Date	Saturday, December 07, 2013	Sheet 4 of 20

PMIC

With low-inductive paths between VIN the voltage sources, either 0.22 uF or 0.47 uF may be used.

1.375 V Hardware Default for Boot



BOM Deviation - Change R26 from 10 kohm to 100 kohm to comply with PMIC data sheet.

VDDOTP Programming Mode External Power - Remove pull-up resistor, install series resistor, and connect test point to 8 volts to program PMIC fuses.

For mass production, Freescale strongly recommends tying VDDIO to P3V3_DELAYED to eliminate backfeed from the I2C port during power-up.

Peripheral Power Rails

Voltage (V)	Rail Name	Block	Power Source	Generated By	Current Capability (A)
12	VBAT	MLB	Wall Supply	MB	5.5
5	P5V0_DELAYED	Para LCD	Main Power	MB or Jack	0.5
		LVDS LCD			
		HDMI			
5	P5V0_OTG_VBUS	USB	switcher	MB	0.8
		USB			
3.3	P3V3_DELAYED	NAND Flash	switcher	LT3680	3.5
		SD Card			
		NOR Flash			
		HDMI			
		LVDS LCD			
		Ethernet			
		UART			
		MIPI			
		Mini PCIE			
		MLB (MOST)			
3.0	P3V0_VDD_USB	USB	VDDUSB_CAP	IMX	-
2.8	P2V8_VGEN6	MIPI	VGEN6	PMIC	0.2
1.8	P1V8_SW4	MIPI	SW4	PMIC	1.0
1.5	P1V8_VGEN4	SD Card	VGEN4	PMIC	0.35
1.5	P1V5_DDR_SW3	DDR	SW3A/B	PMIC	2.5
1.5	P1V5_VGEN2	Mini PCIE	VGEN2	PMIC	0.25
1.5	ETH_VDDIO_REG	Ethernet	PHY - on-chip	AR8031	-
0.75	POV75_REFDDR	DDR	VREFDDR	PMIC	0.01

MB = Main board 26662

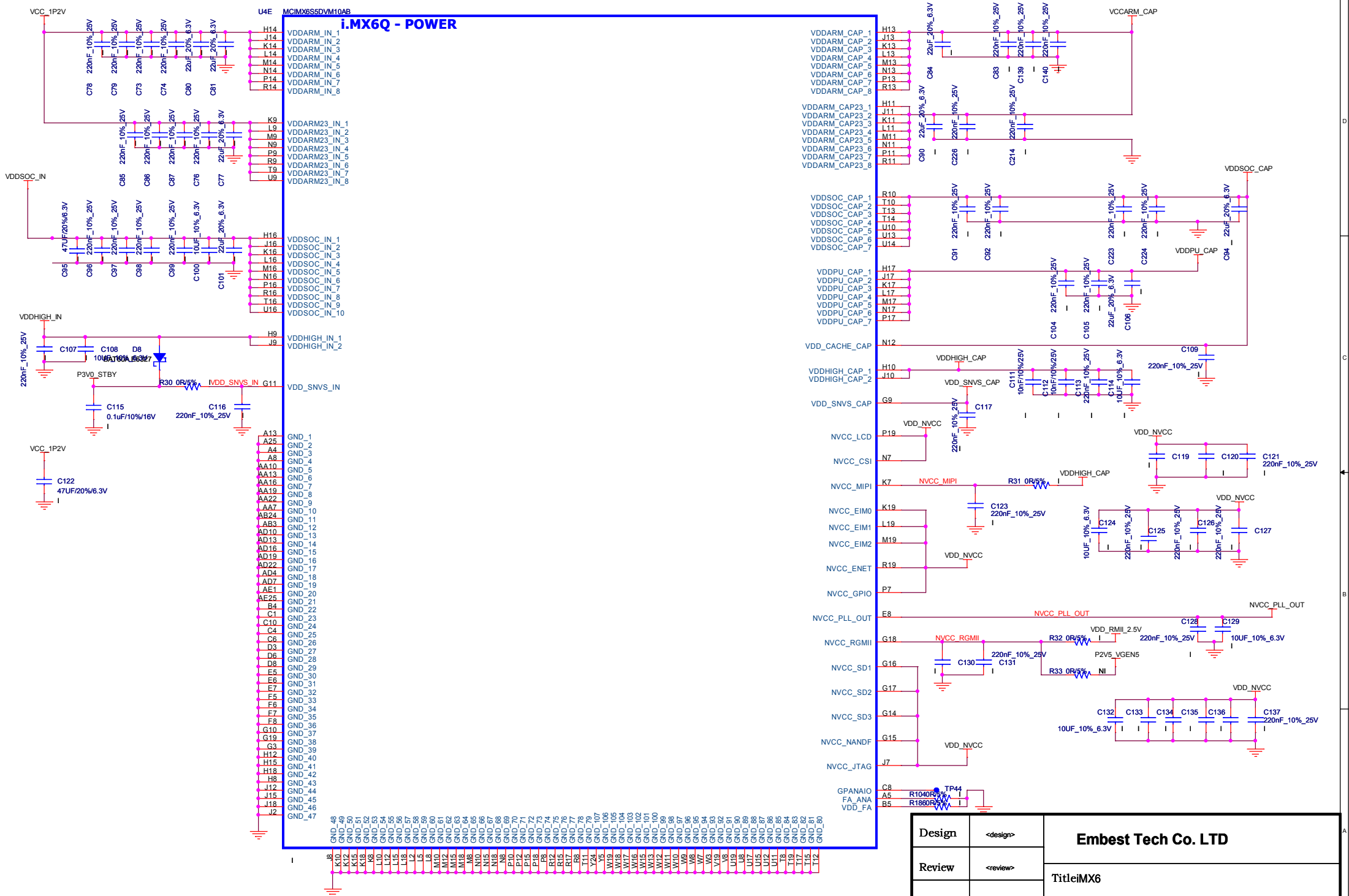
PMIC Output Rails

Regulator	Voltage (V)	Power-Up		Load
		Sequence	Sequence	
VSNVS	3	0	VDD_SNVS_IN	
SW1A/B	1.375	1	VDDARM_IN	
SW1C	1.375	1	VDDSOC_IN	
SW2	3	2	VDDHIGH_IN	
VGEN2	1.5	2	mini PCIE connector	
SW3A/B	1.5	3	NVCC_DRAM, NVCC_RGMII (option)	
SW4	1.8	3	MIPI connector	
VGEN4	1.8	3	NVCC_SD3	
VGEN6	2.8	3	3V3_DELAYED enable, MIPI conn	
VREFDDR	0.75	3	DRAM_VREF	
VGEN5	2.5	3	Pwr LED & 5V0_DELAYED enable	
SWBST	0	N/A	Not used	
VGEN1	0	N/A	Not used	
VGEN3	0	N/A	Not used	

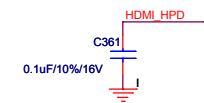
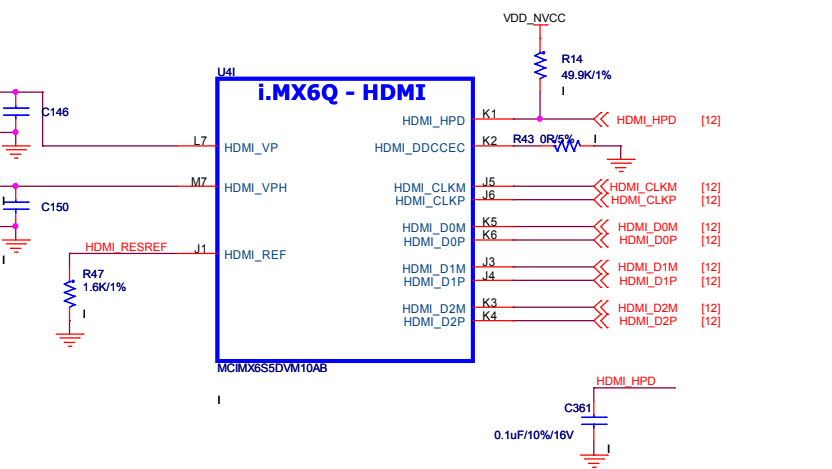
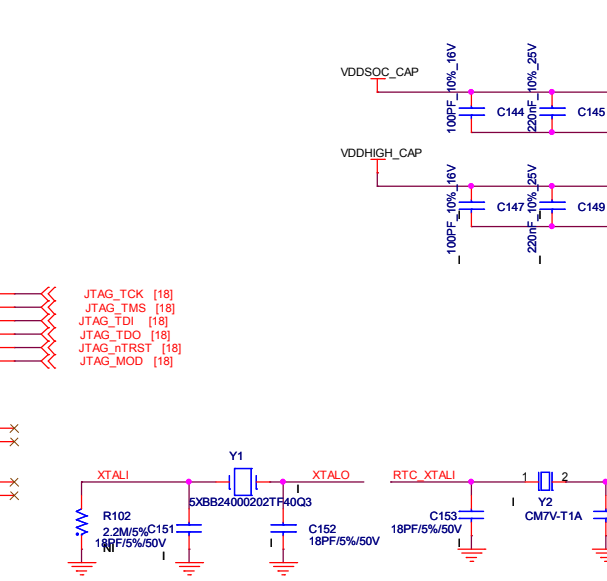
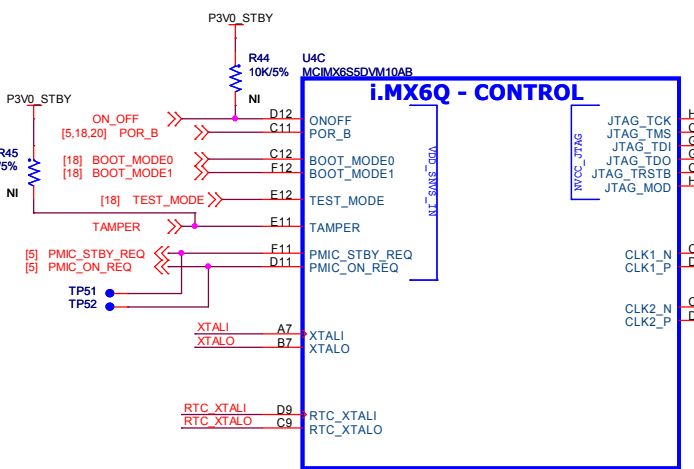
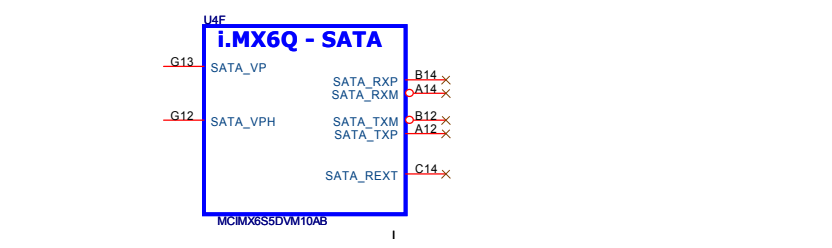
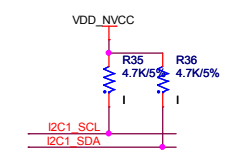
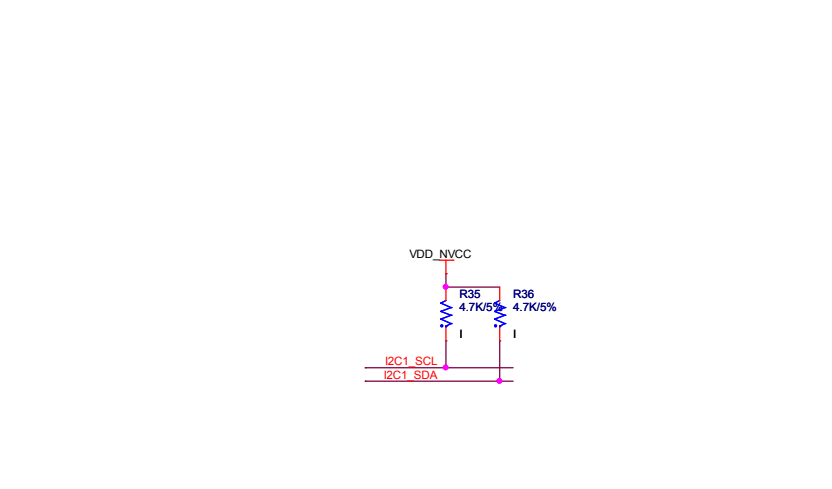
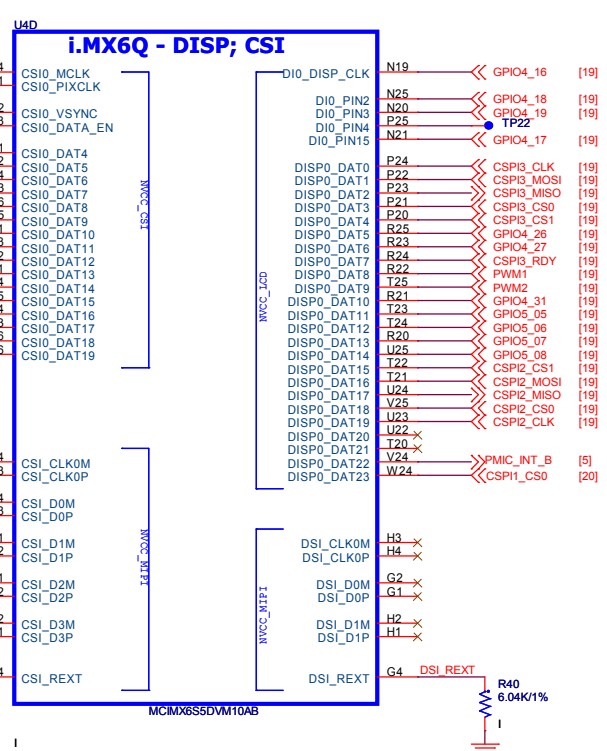
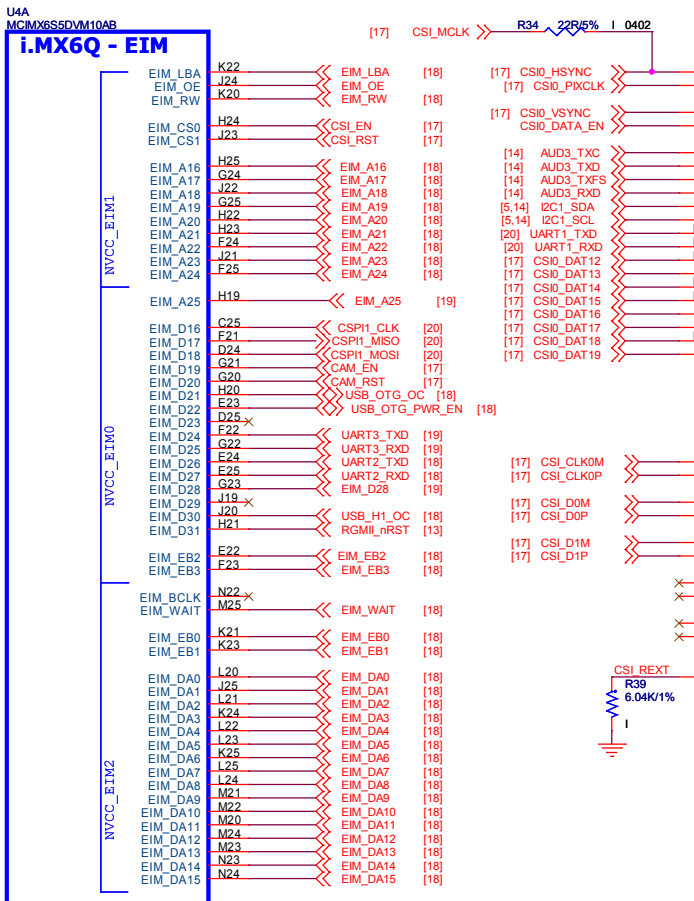
SW1A/B = 1.375 V for boot-up at ~800 MHz. Recommend that software increase SW1A/B to 1.425 V for 1 GHz operation.

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Standardize	<standardize>	Date	Saturday, December 07, 2013	Sheet 5 of 20

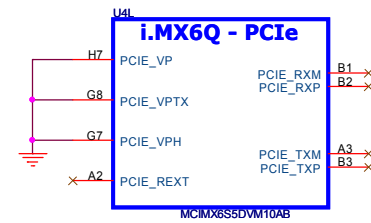
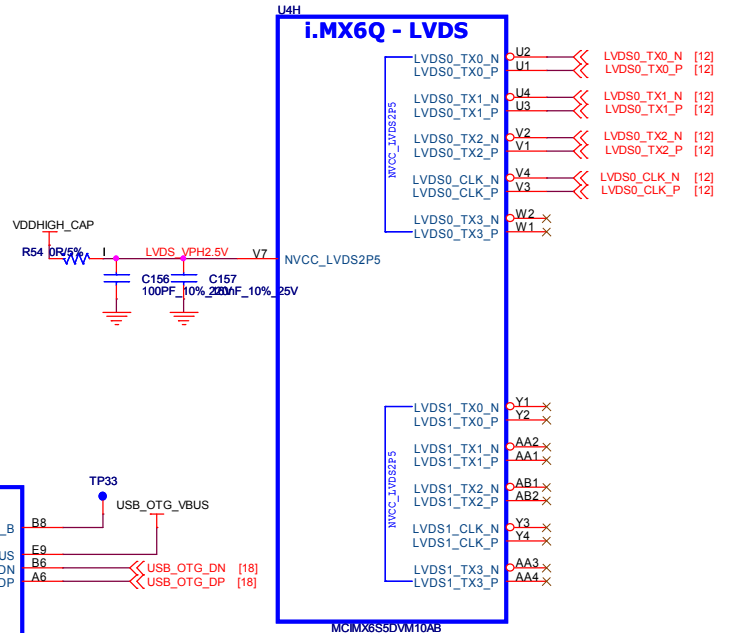
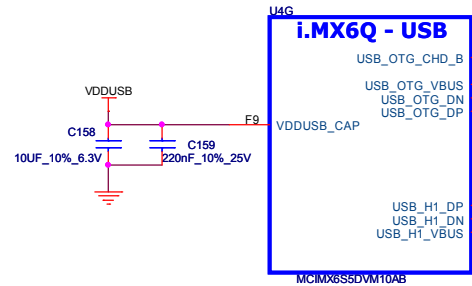
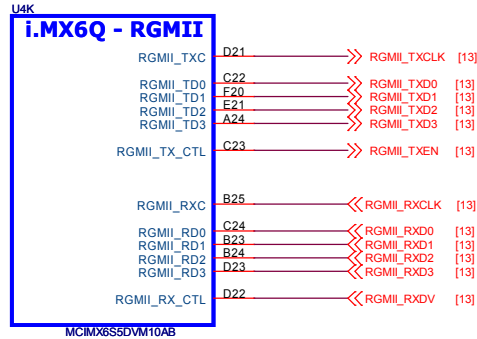
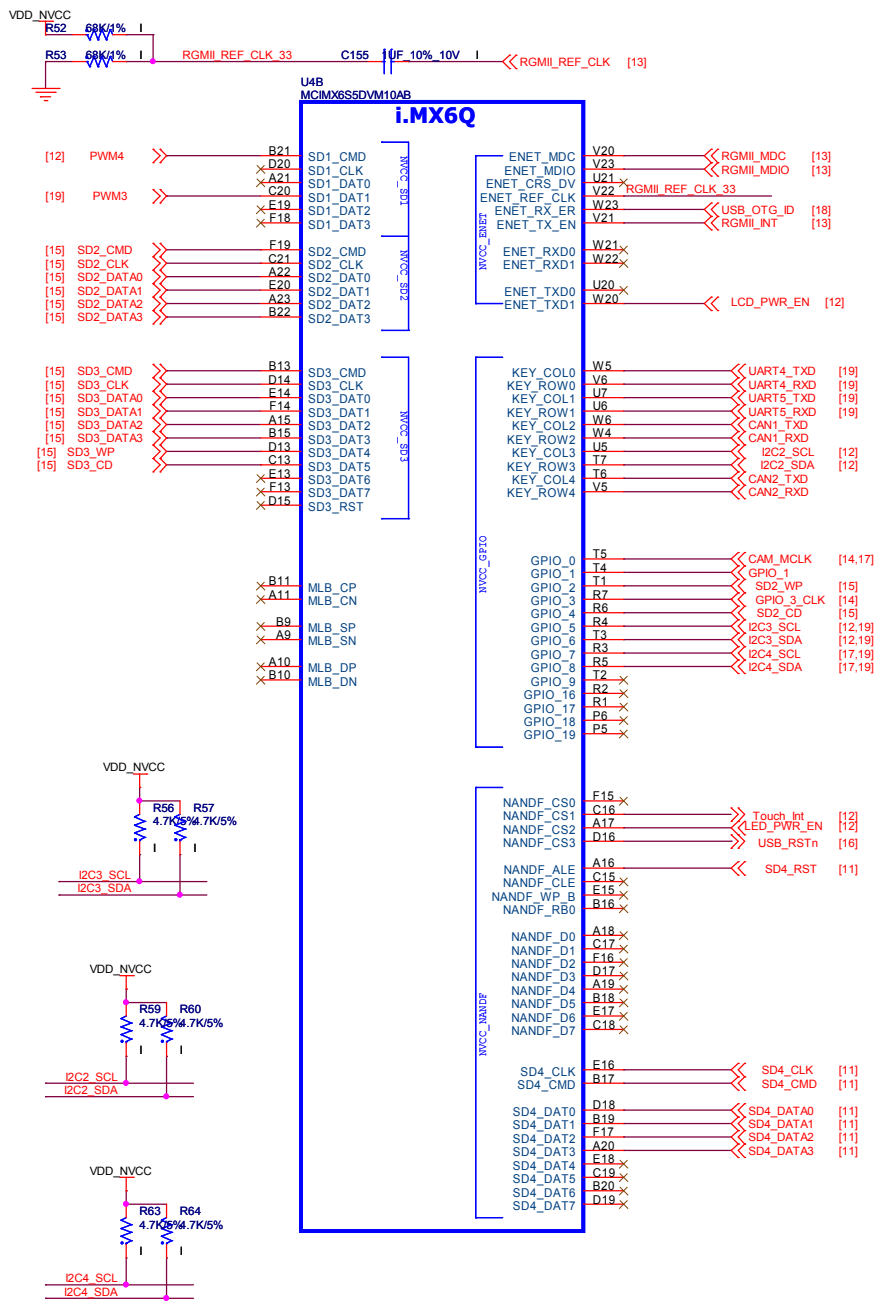
I.MX6Q - POWER



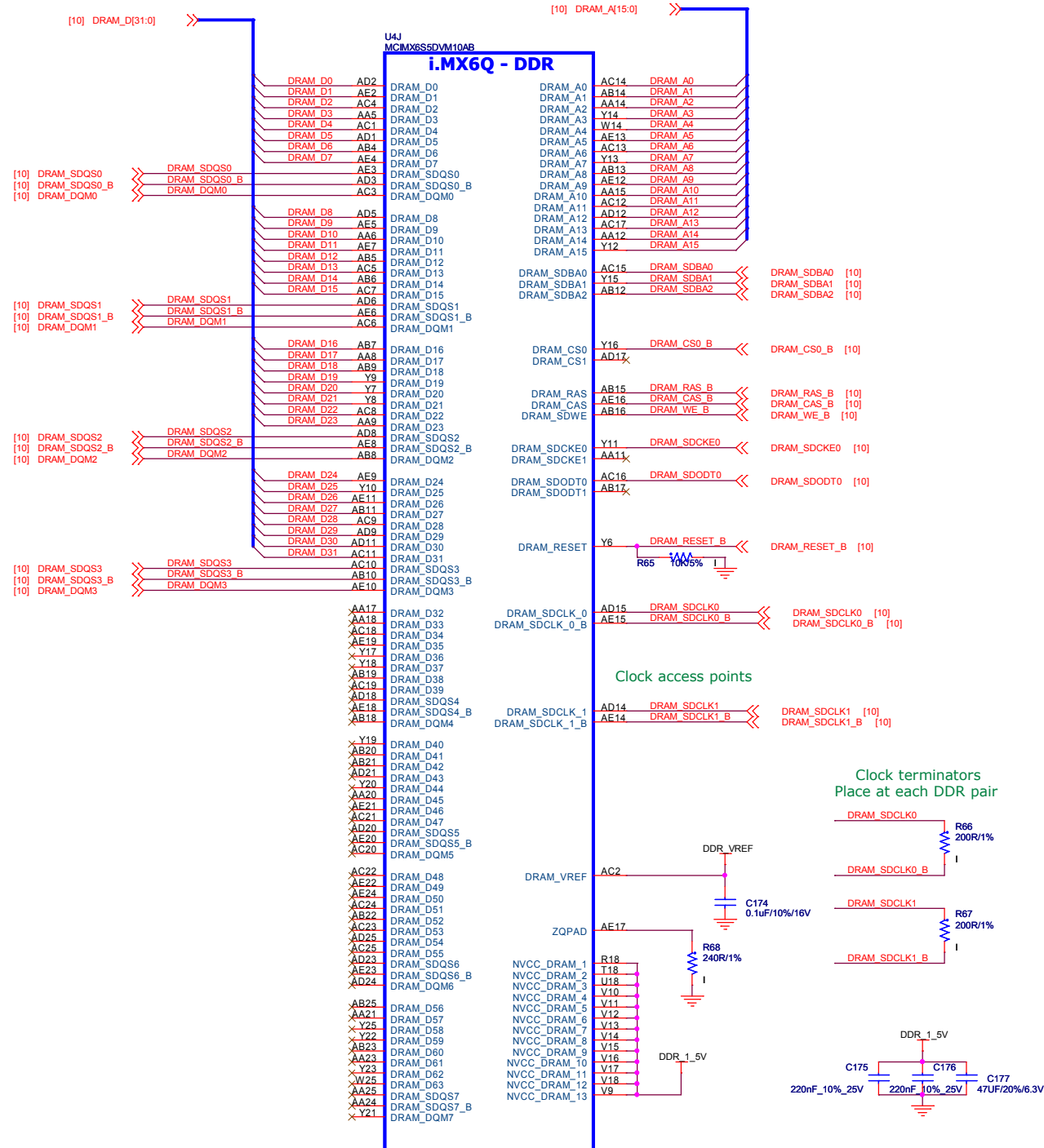
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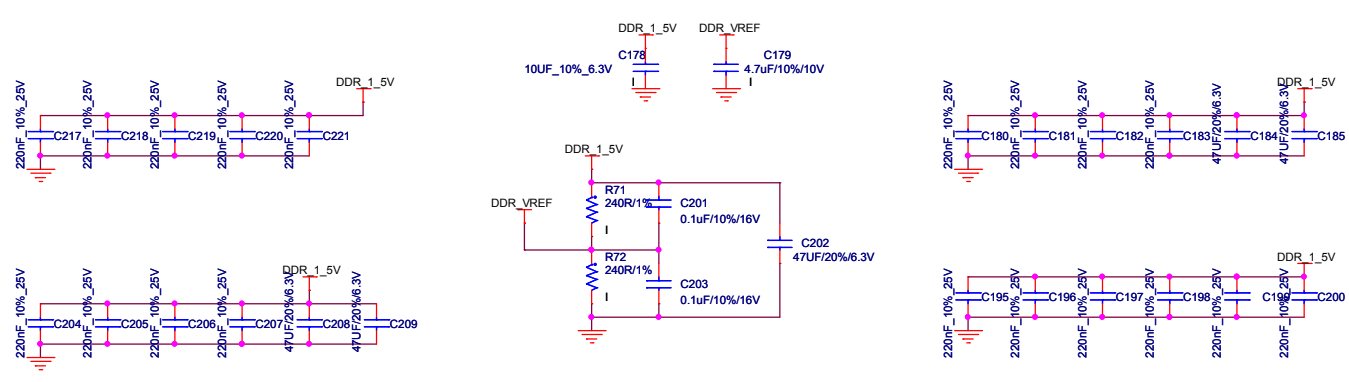
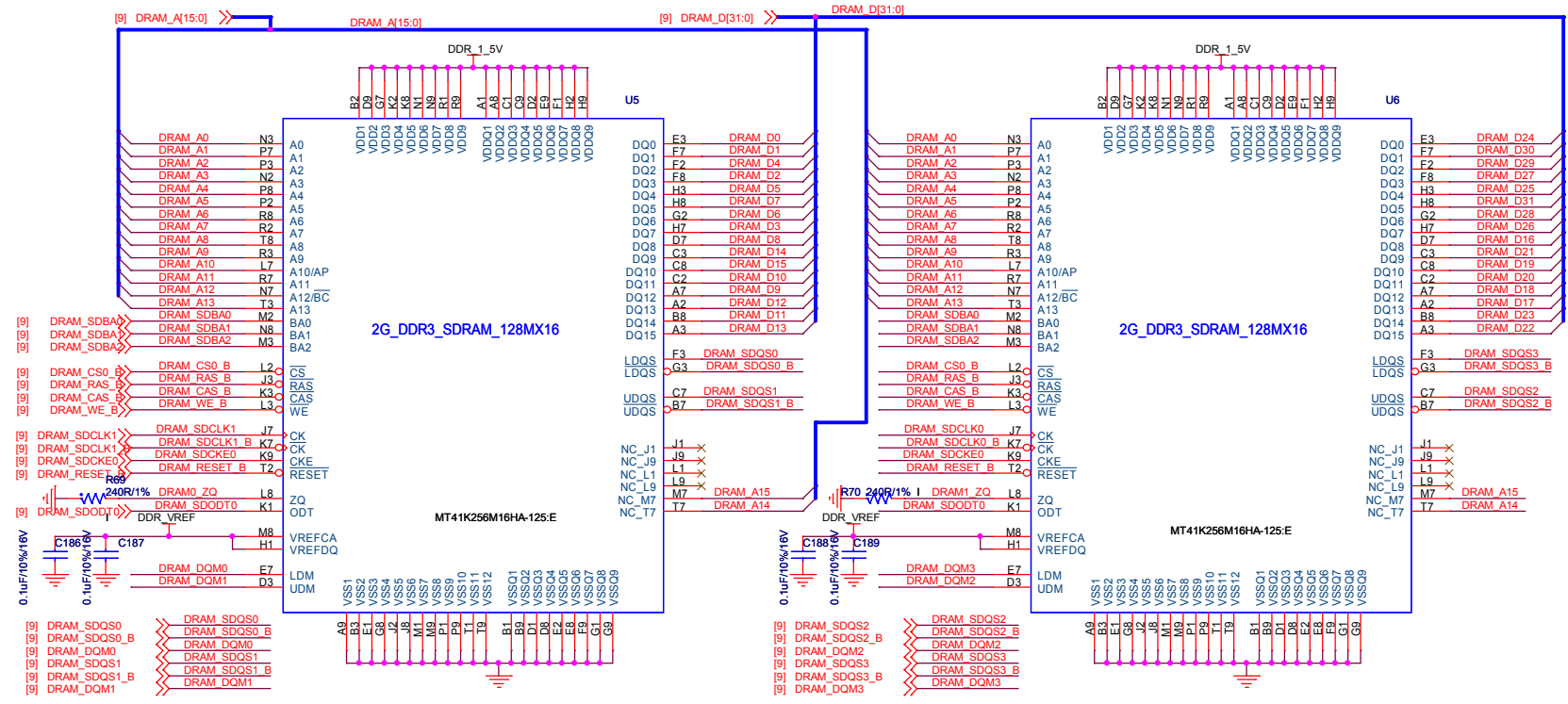
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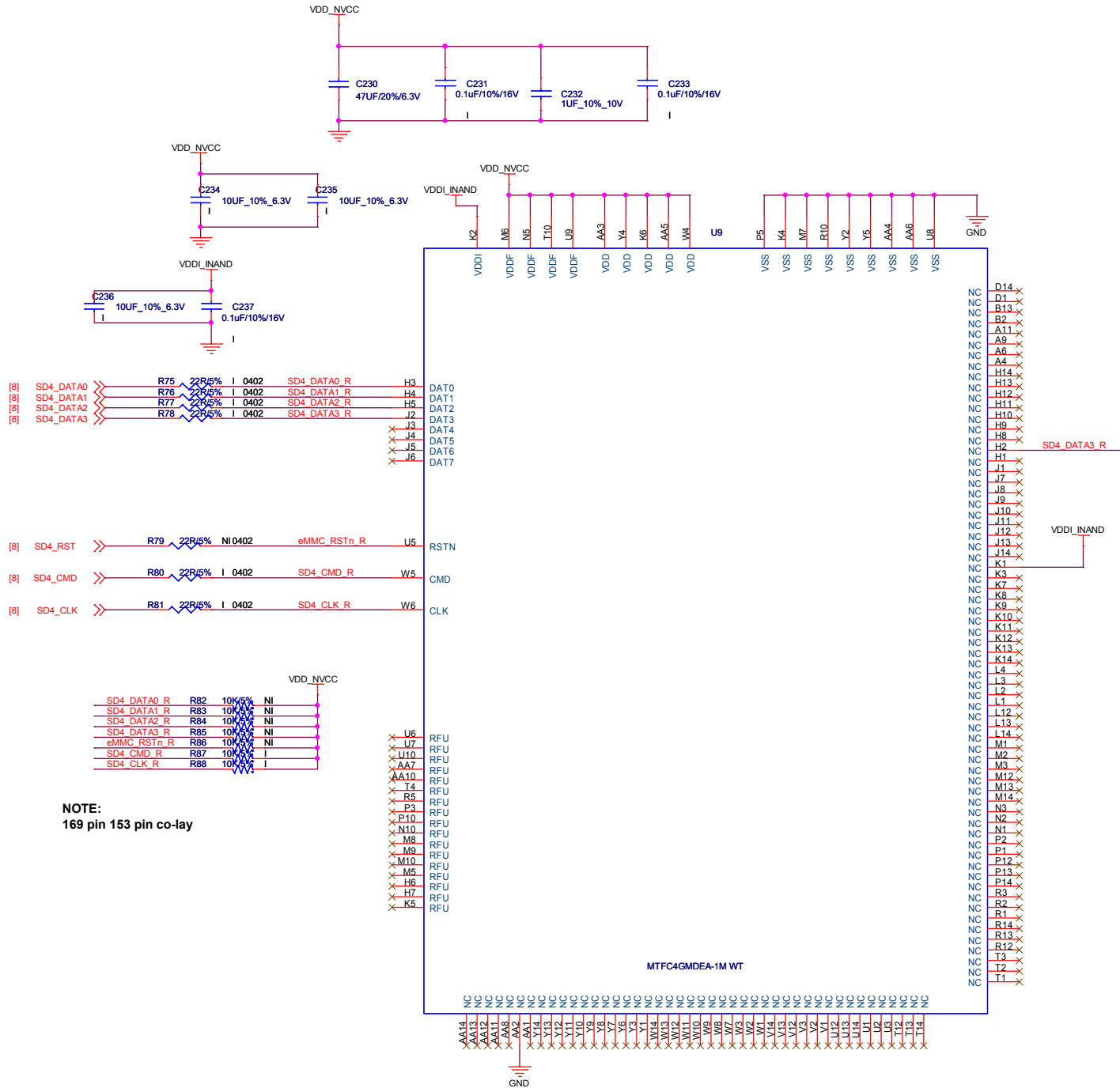
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		Date	Monday, December 09, 2013	Sheet 9 of 20



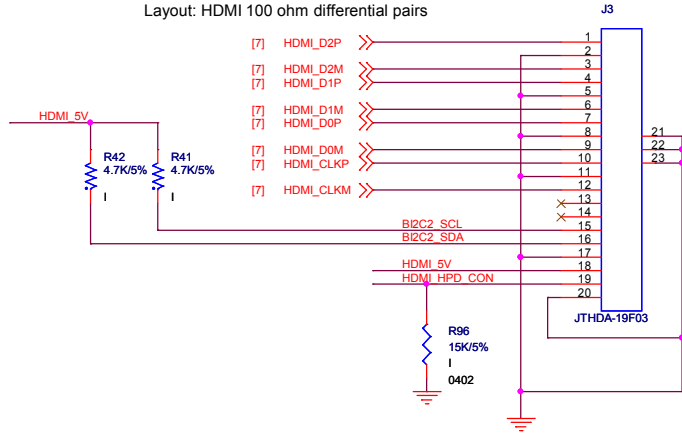
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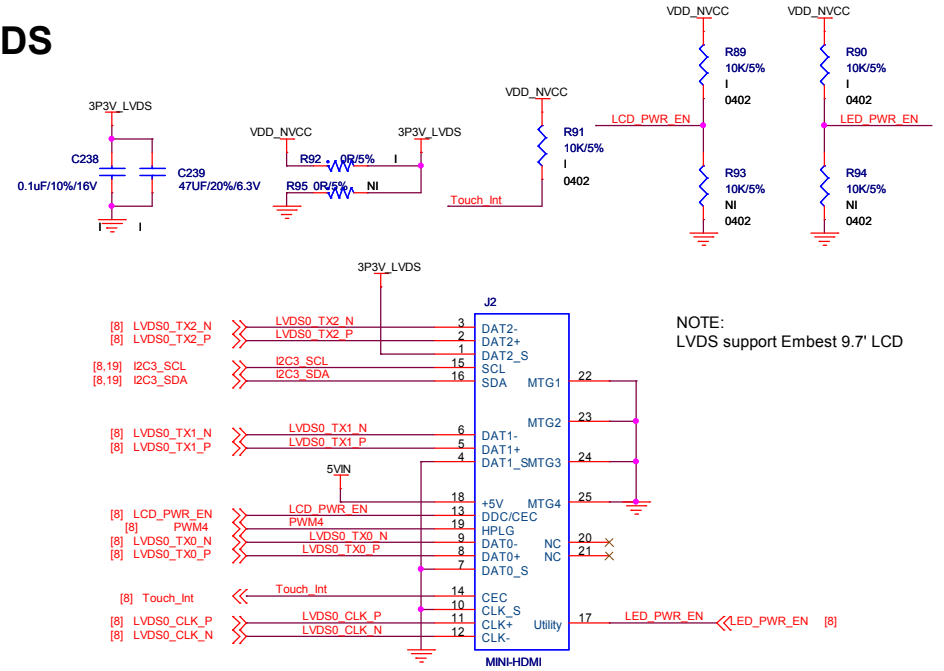
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Size	Document Number	Rev
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Date:	Saturday, December 07, 2013	Sheet 11 of 20

HDMI

Layout: HDMI 100 ohm differential pairs

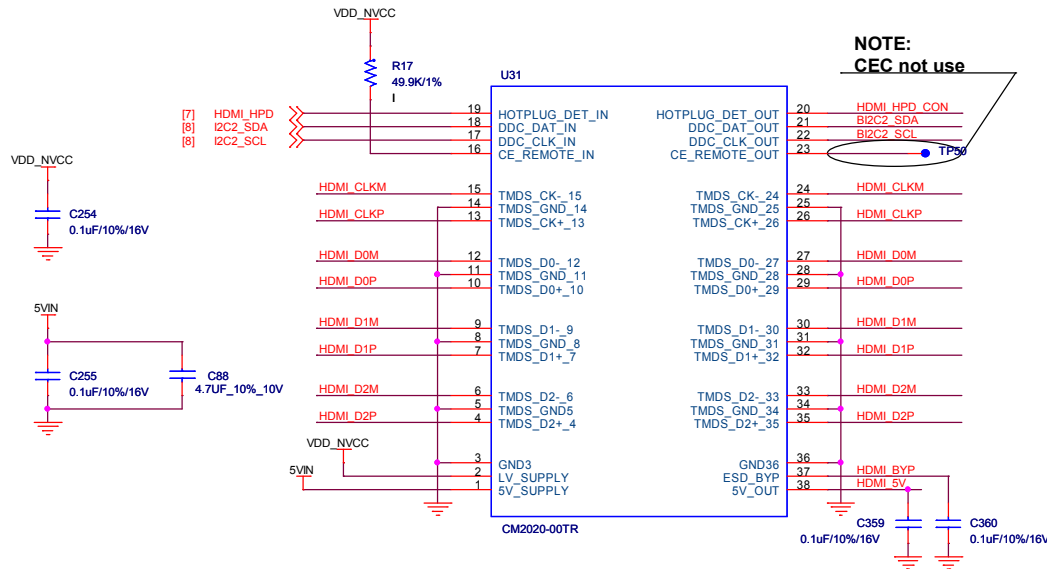


LVDS



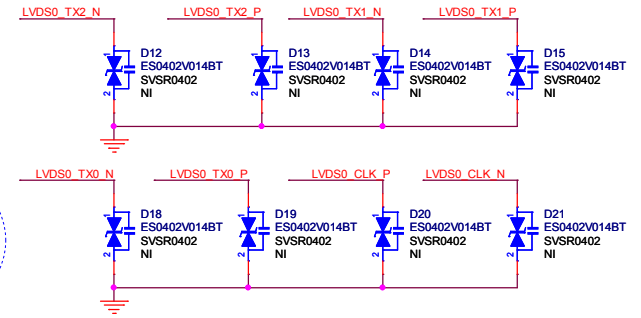
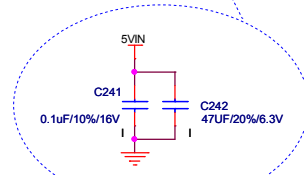
NOTE:
LVDS support Embest 9.7" LCD

HDMI ESD Protected



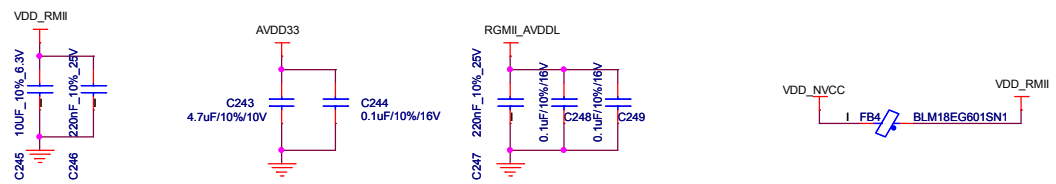
NOTE:
CEC not use

NOTE:
Close to J2 pin18

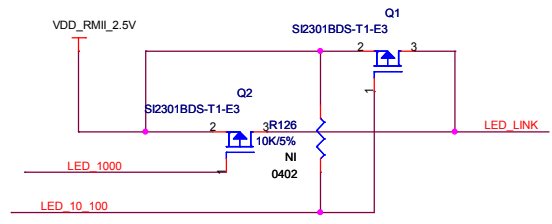
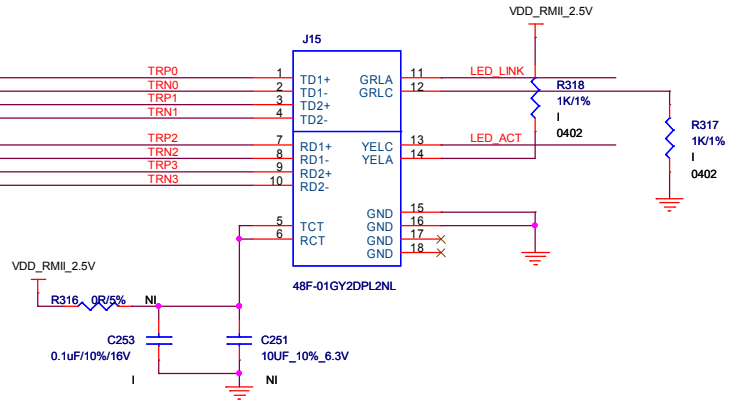
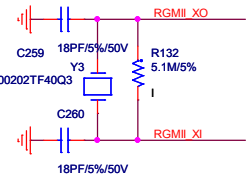
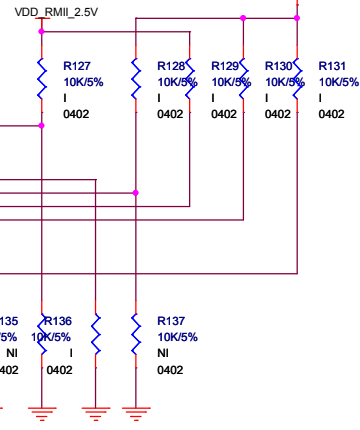
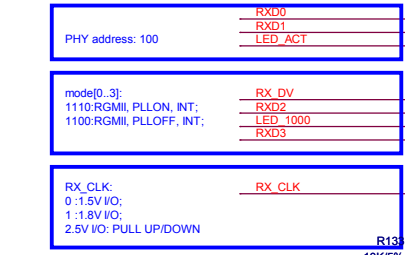
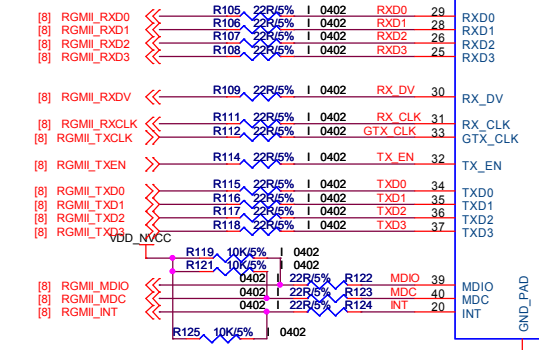
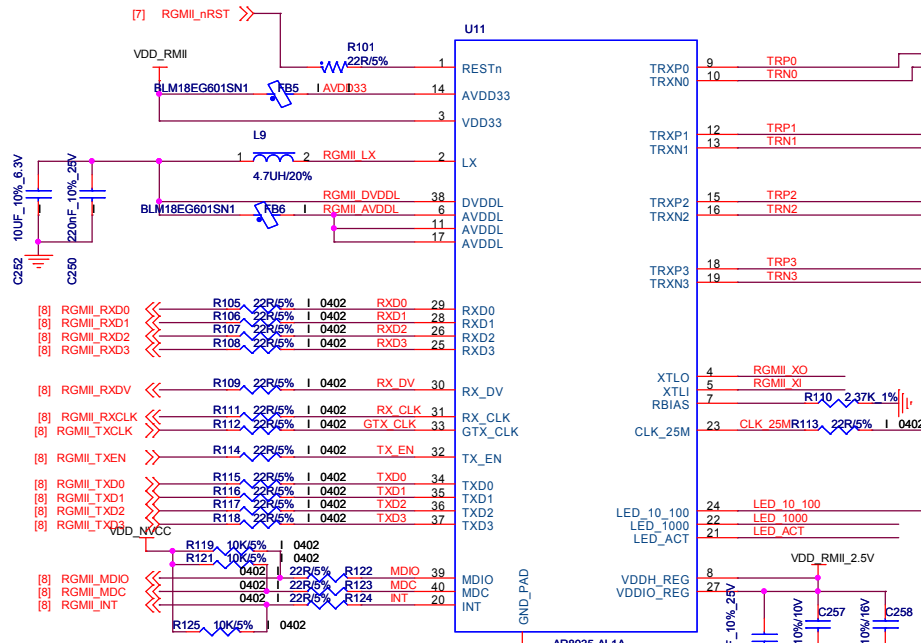


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LAN



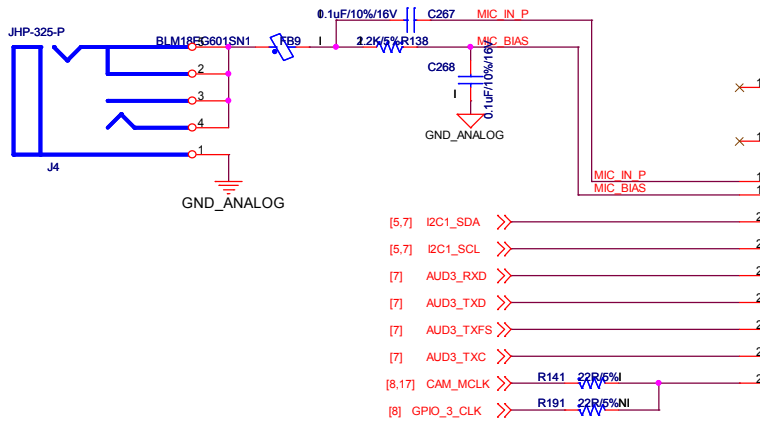
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Put the 22ohm resistors in this page near imx6



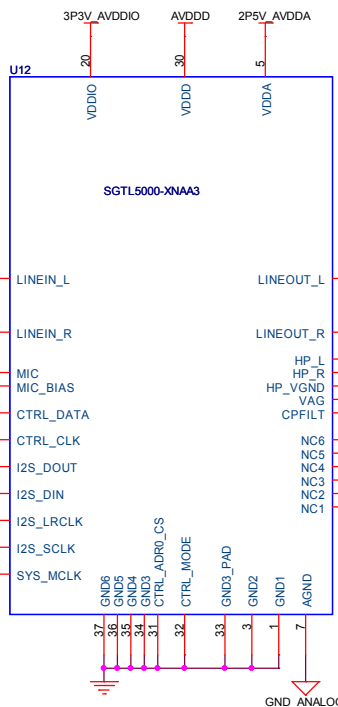
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		Date: Saturday, December 07, 2013	Sheet 13 of 20	

AUDIO

MIC IN

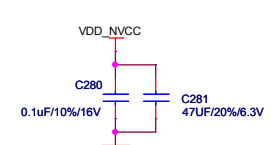
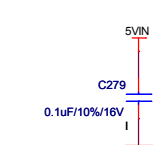
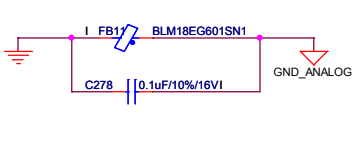
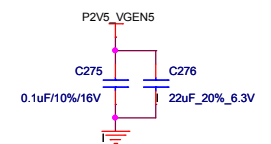
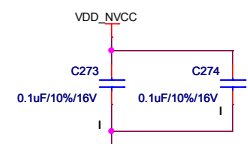
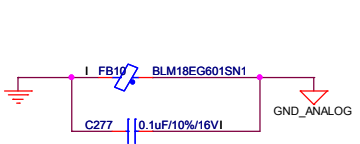
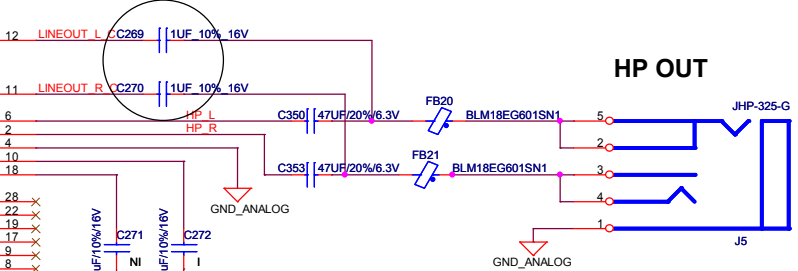


- [5,7] I2C1_SDA >>
- [5,7] I2C1_SCL >>
- [7] AUD3_RXD >>
- [7] AUD3_TXD >>
- [7] AUD3_TXFS >>
- [7] AUD3_TXC >>
- [8,17] CAM_MCLK >> R141 22R/5% I
- [8] GPIO_3_CLK >> R191 22R/5% NI



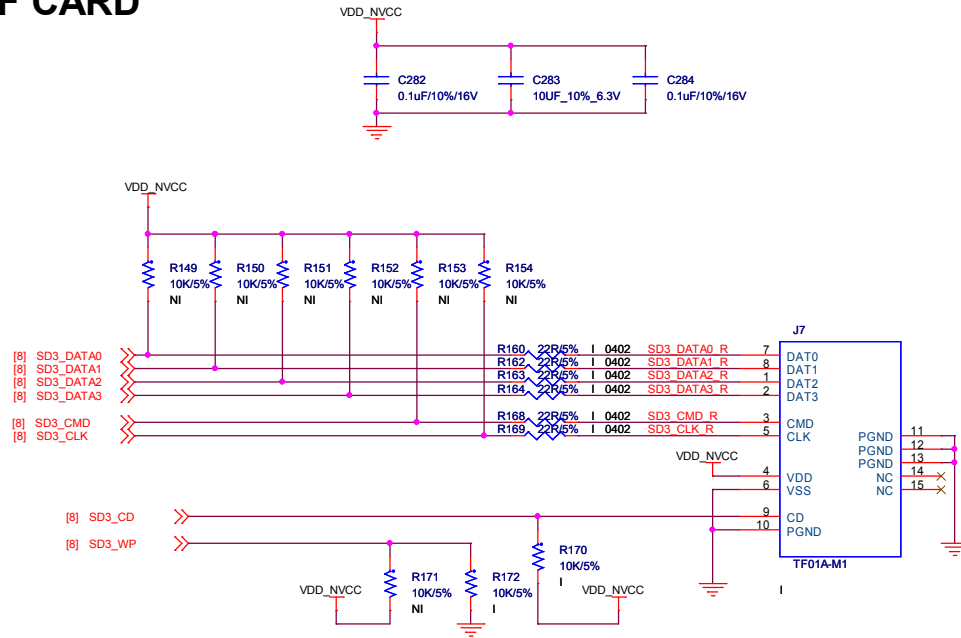
NOTE:
Line out reserve
NI in MP

HP OUT

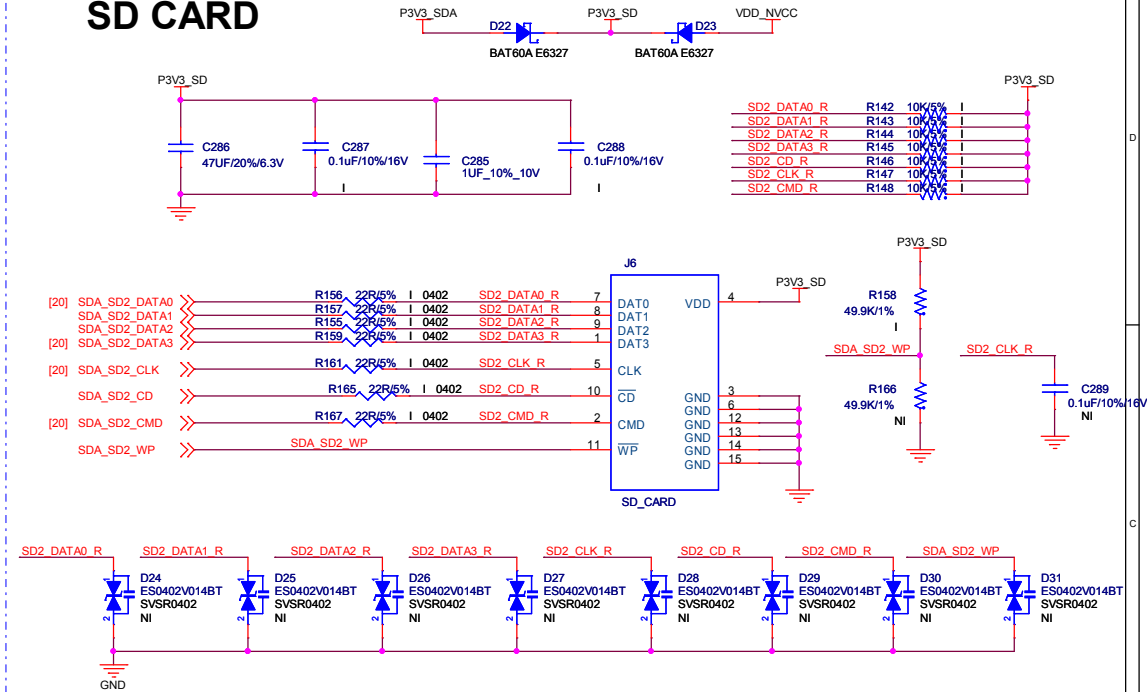


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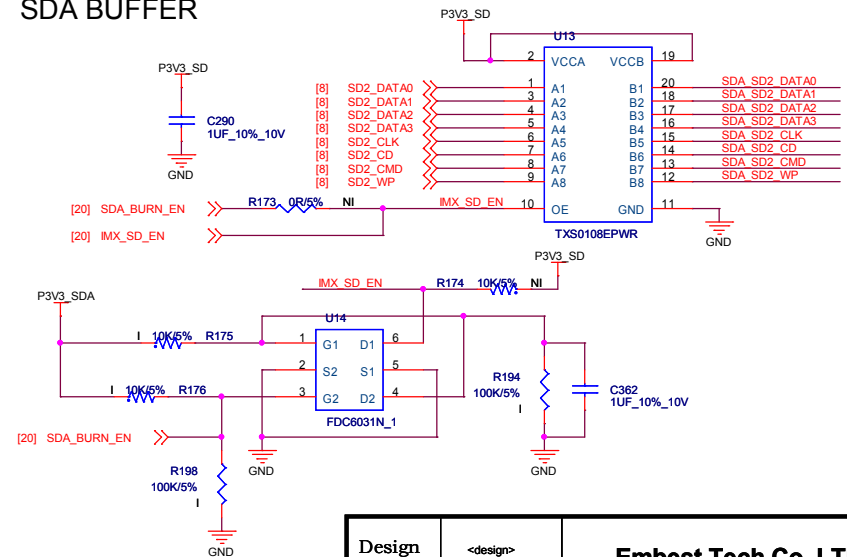
TF CARD



SD CARD

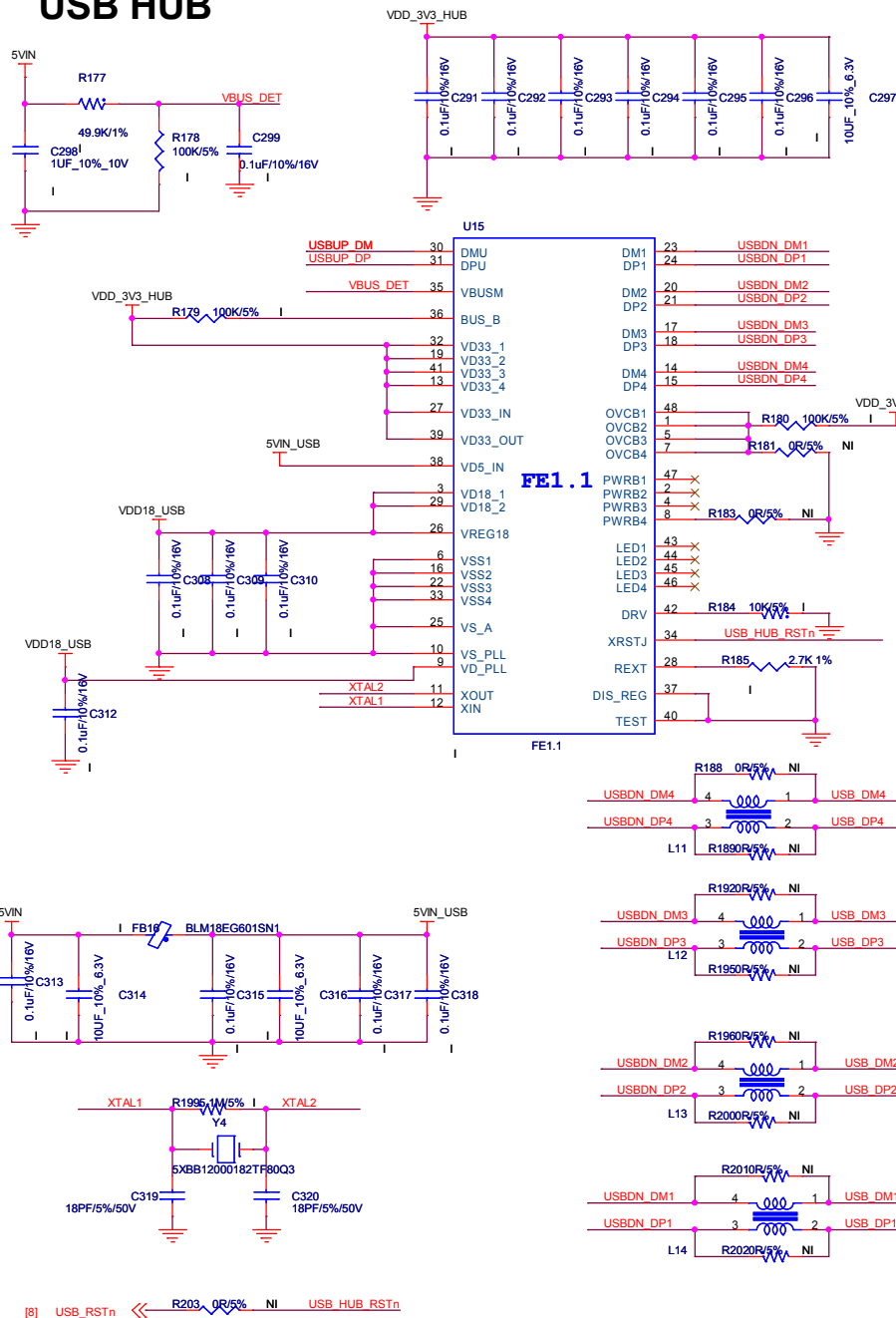


SDA BUFFER



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		A3	15 SD/MMC	V1.0
		Date	Monday, December 09, 2013	Sheet 15 of 20

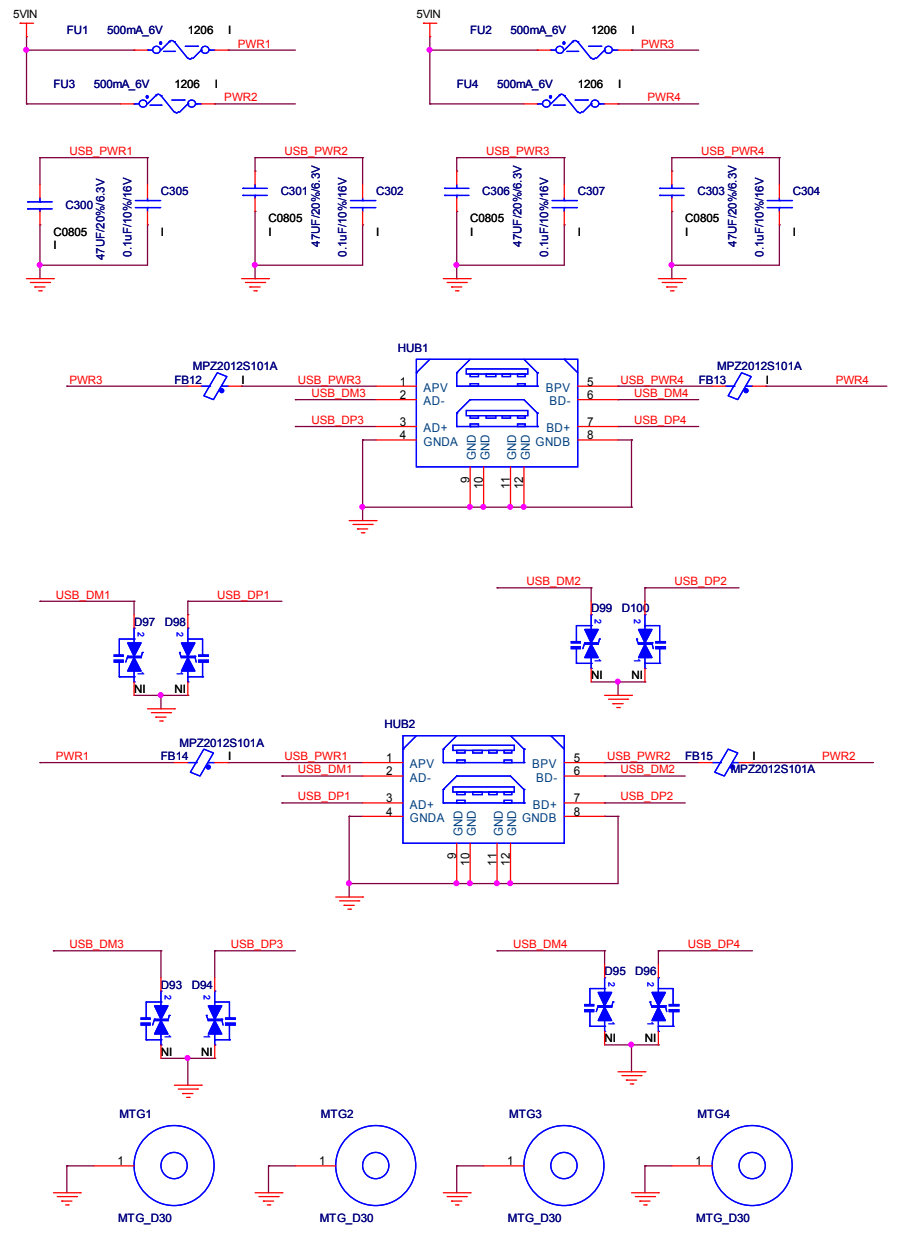
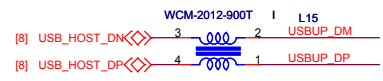
USB HUB



FE1.1

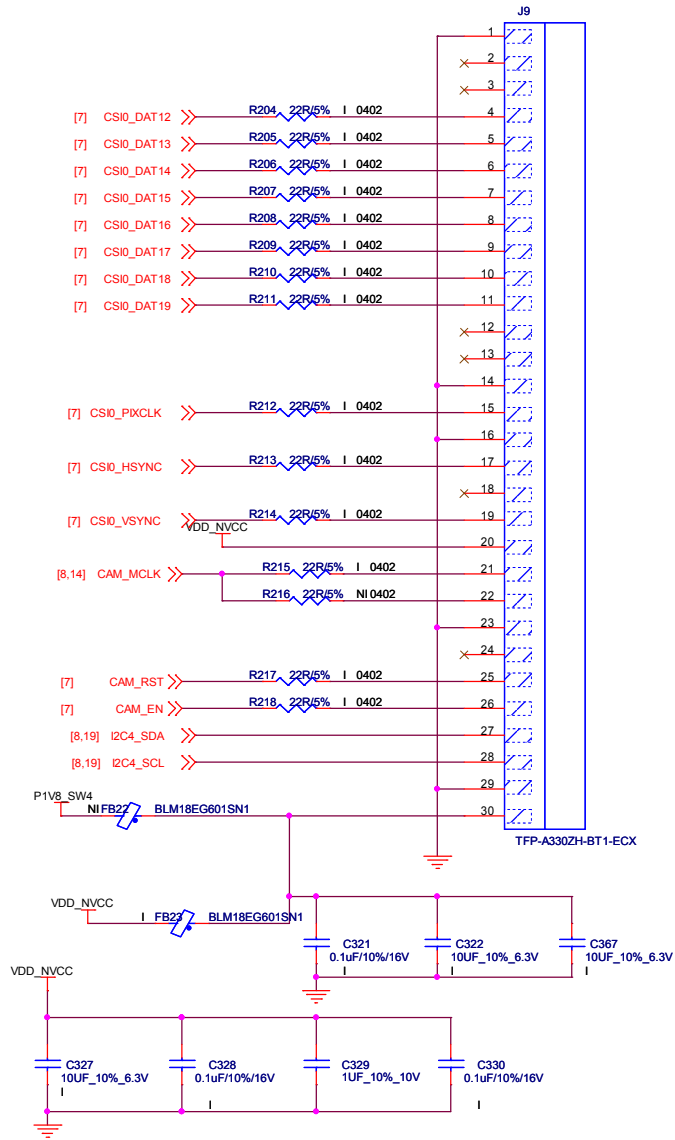
FE1.1

USB Up Stream

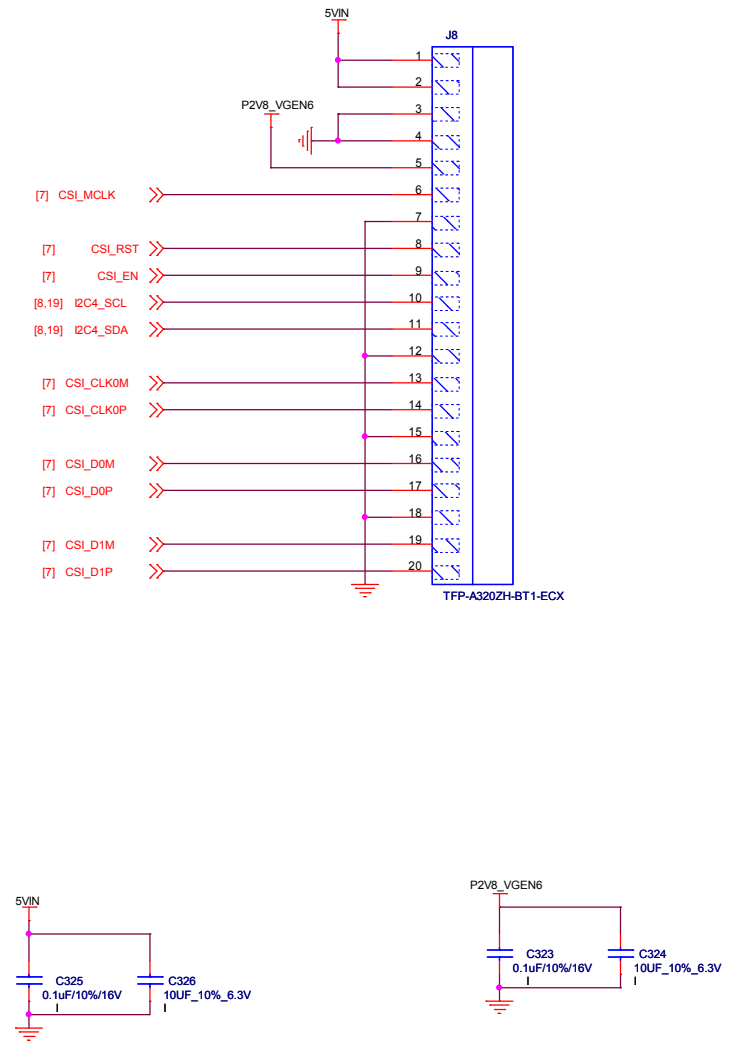


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		Date: Saturday, December 07, 2013	Sheet: 16 of 20	

Parallel

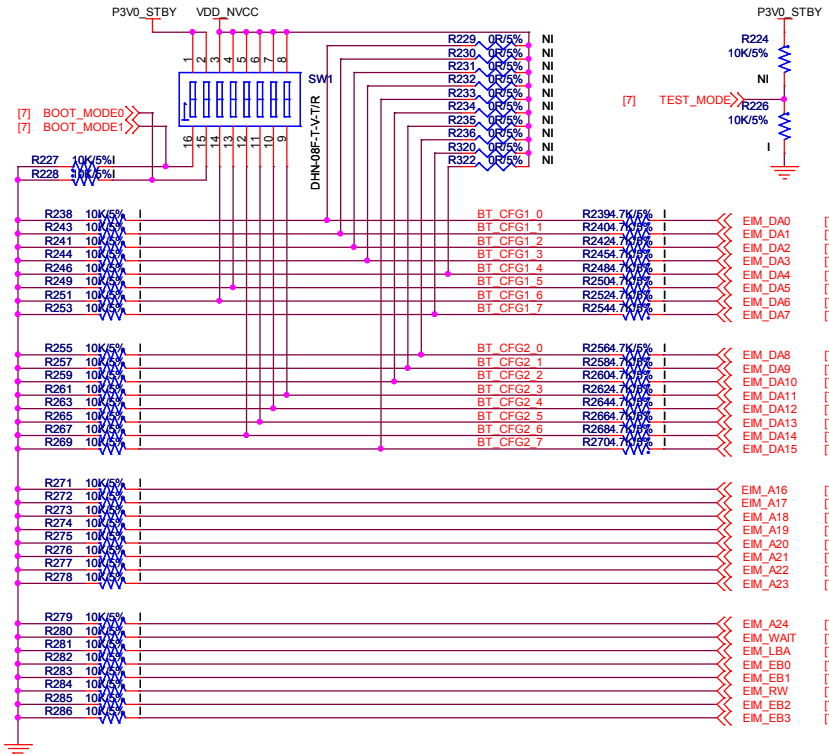


CSI



Design	<design>	Embest Tech Co. LTD		
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BOOT DEV



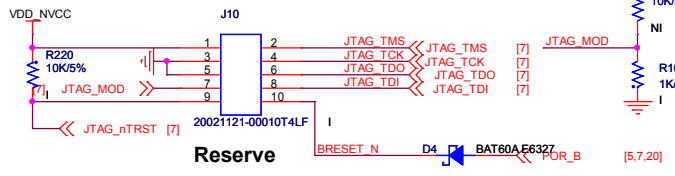
NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilities include:
1) As close to processor as possible.
2) Close to other components using EIM signals.
iMX solo don't support SATA feature

Table 7-1. Boot MODE Pin Settings

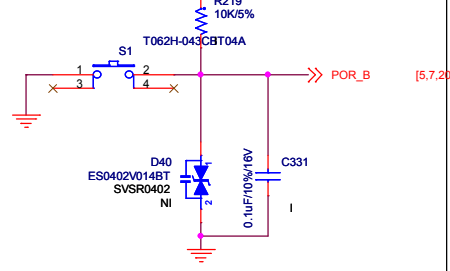
BOOT_MODE[1:0] ¹	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

1. BOOT_MODE[1:0] <- {BOOT_MODE1,BOOT_MODE0} (at rising edge of RESET_B)

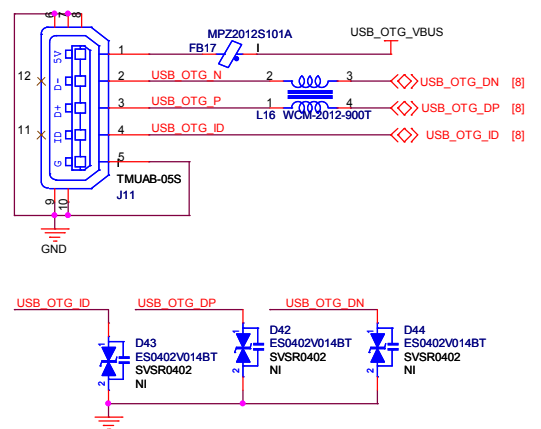
JTAG



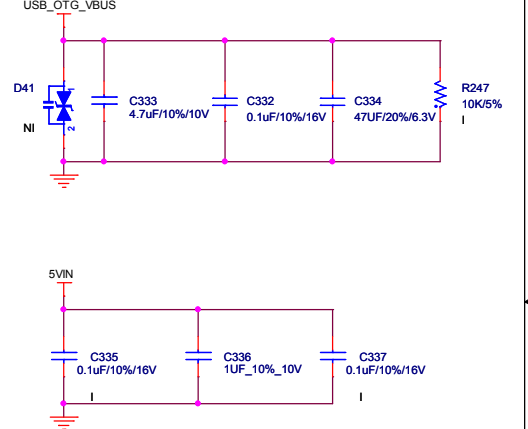
RESET



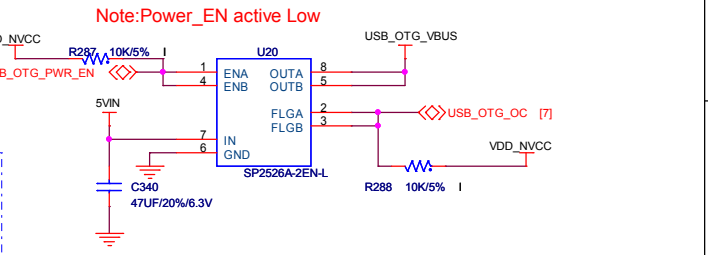
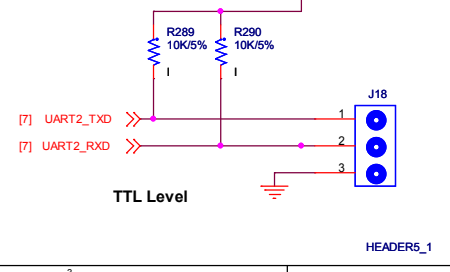
USB OTG



BOOT MODE



UART2

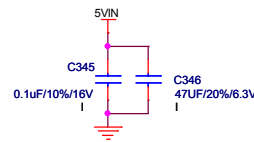
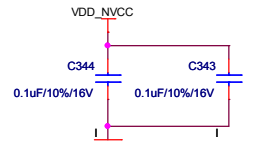
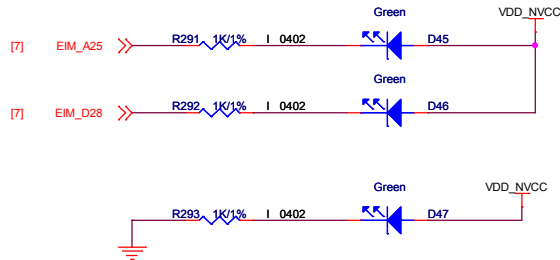
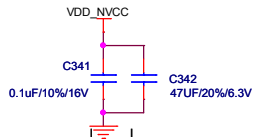
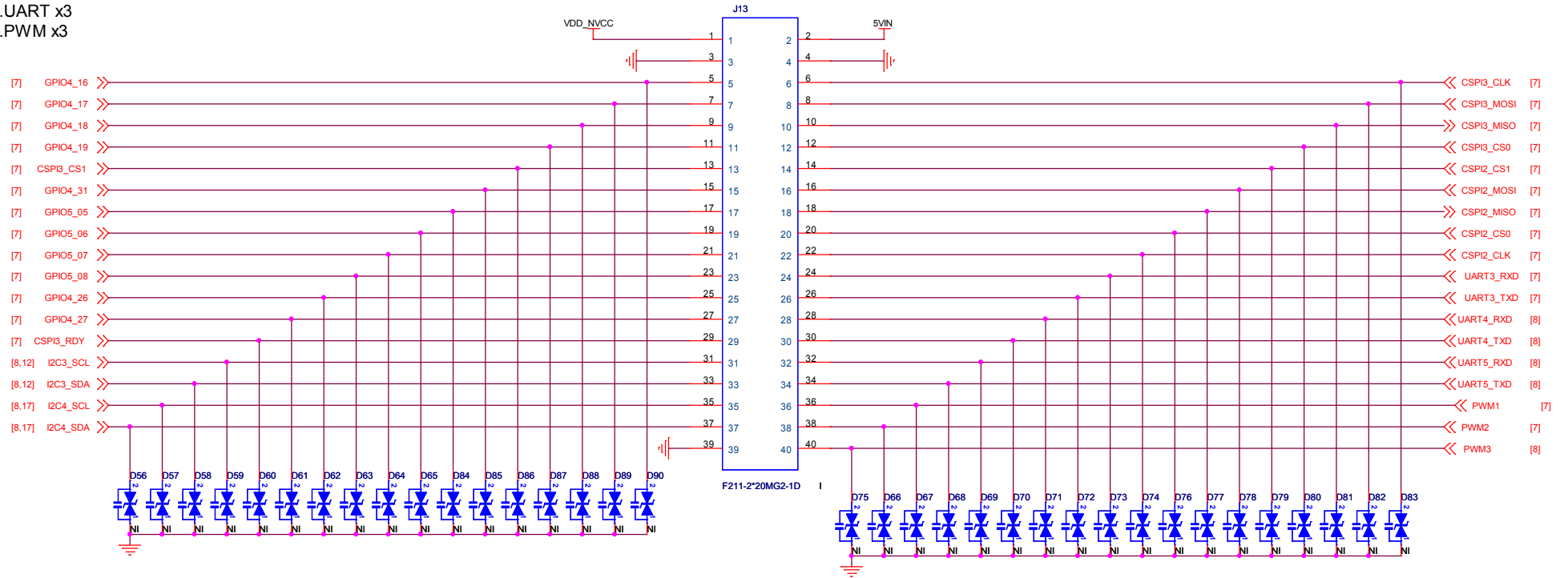


Design	<design>	Embtest Tech Co. LTD		
Review	<review>			
Authorize	<authorize>	Title iMX6		
Standardize	<standardize>	Size A3	Doc Name 18 BOOT/UART2	Ver. V1.0
		Date Wednesday, January 15, 2014	Sheet 18 of 20	

Expantion Port

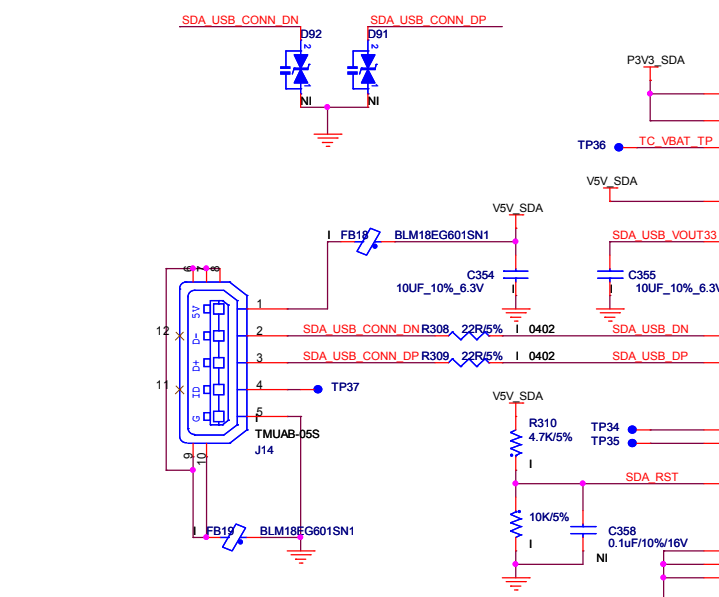
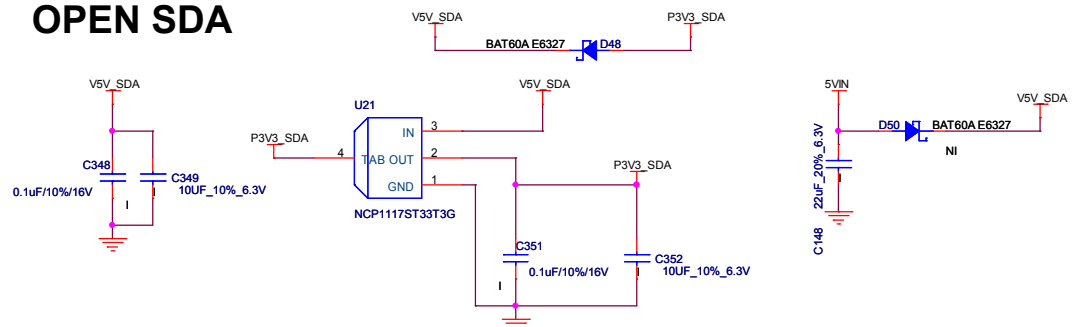
Expantion port include:

- 1.20bits RGB
- 2.I2C x2
- 3.SPI x2
- 4.UART x3
- 5.PWM x3

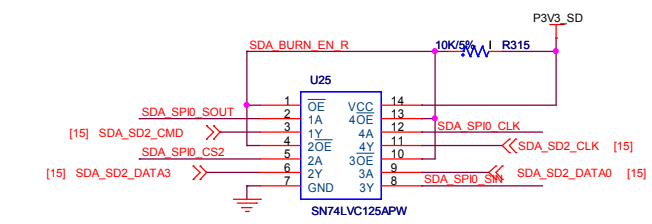


Design	<design>	Embest Tech Co. LTD		
Review	<review>			
Authorize	<authorize>	Title:MX6		
Standardize	<standardize>	Size	Doc Name	Ver.
		A3	19 EXPANSION PORT	V1.0
		Date	Saturday, December 07, 2013	Sheet 19 of 20

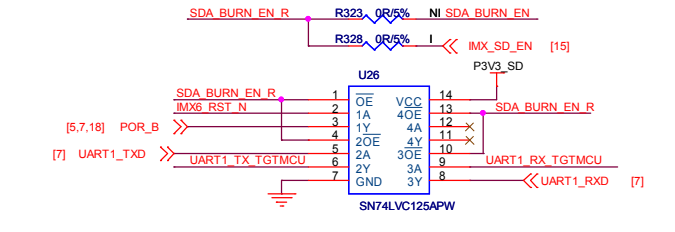
OPEN SDA



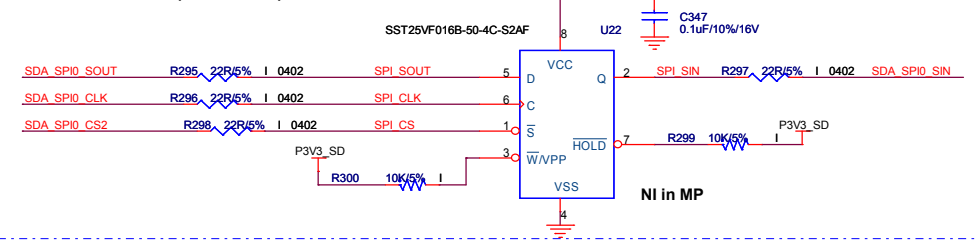
Pin #	SD Mode			SPI Mode		
	Name	Type ¹	Description	Name	Type ¹	Description
1	CD/DAT3 ⁴	I/O/PP ²	Card Detect/ Data Line [BIT 3]	CS	I ¹	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [BIT 0]	DO	O/PP	Data Out
8	DAT1 ⁴	I/O/PP	Data Line [BIT 1]	RSV		
9	DAT2 ²	I/O/PP	Data Line [BIT 2]	RSV		



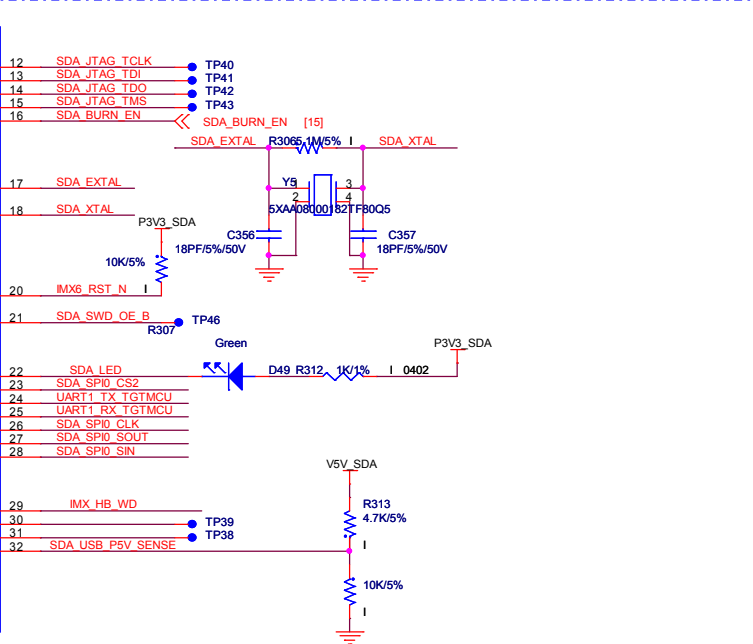
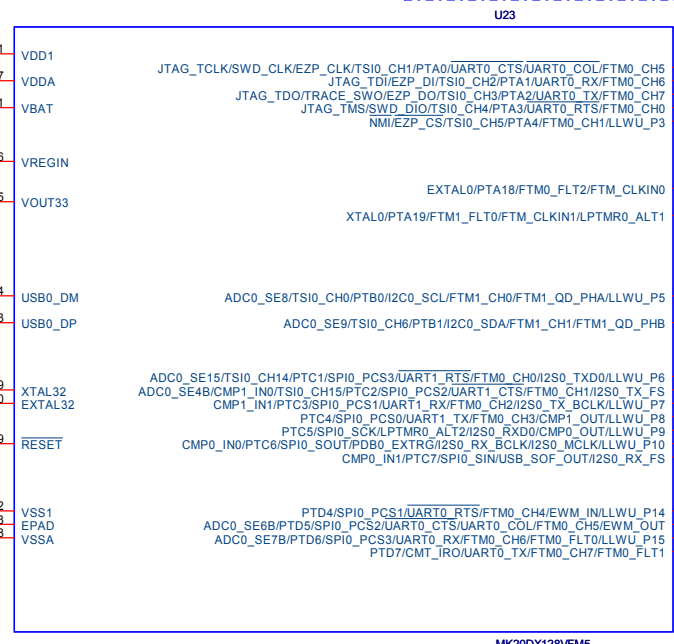
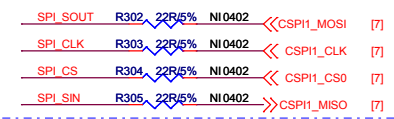
SDA_MCU BUFFER



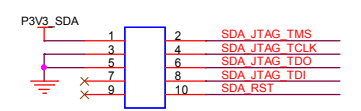
SPI FLASH (reserve)



Reserve for debug



Reserve



Design	<design>	Embest Tech Co. LTD		
Review	<review>			
Authorize	<authorize>	Title: MX6		Ver. V1.0
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		Date: Saturday, December 07, 2013	Sheet: 20 of 20	