# Programmable Charge Pump

- +5V Only Low Power Voltage Conversion
- Programmable Between ±5V or ±10V
- Low Power Shutdown Mode

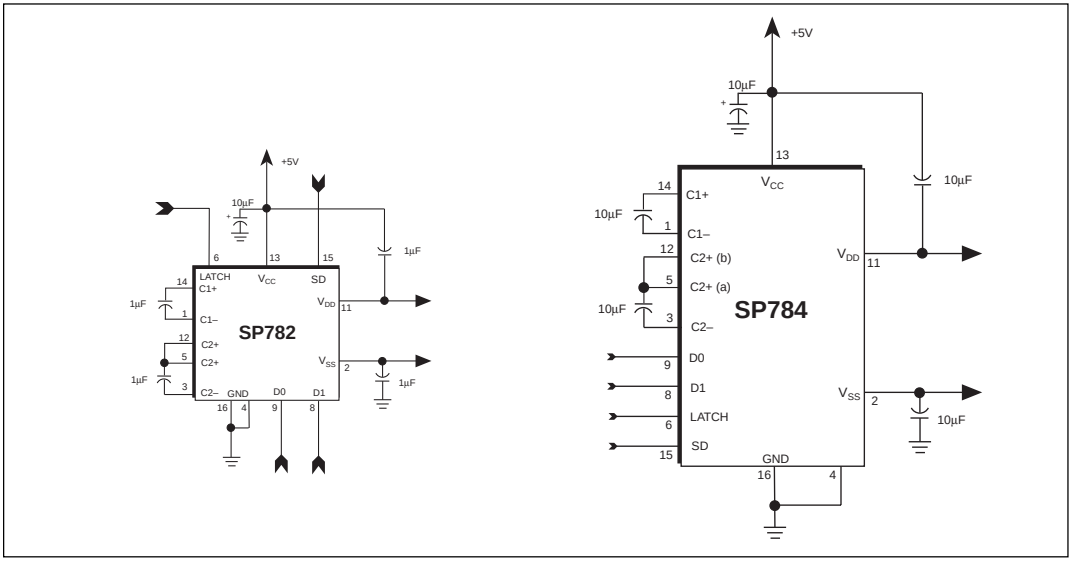
Applications

- RS-232/RS-423 transceiver power supplies
- LCD BIAS Generator
- OP-Amp Power Supplies


## DESCRIPTION...

The **SP782** and **SP784** are monolithic programmable voltage converters that produce a positive and negative voltage from a single supply. The **SP782** and **SP784** are programmable such that the charge pump outputs either a ±10V voltage or a ±5V voltage by control of two pins. Both products require four (4) charge pump capacitors to support the resulting output voltages. The charge pump architecture (U.S. 5,760,637) is fabricated using a low power BiCMOS process technology.

The **SP782** and **SP784** charge pumps can be powered from a single +5V supply. The low power consumption makes these charge pumps ideal for battery operated equipment. Both offer a shutdown feature that saves battery life. A system can essentially have four (4) different supply voltages from a single battery. Typical applications are handheld instruments, notebook and laptop computers, and data acquisition systems.



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$.....+7V
$V_{DD}$.....+11V
$V_{SS}$.....–11V
Storage Temperature.....-65˚C to +150˚C
Power Dissipation
16-pin Plastic DIP.....1000mW
16-pin Plastic SOIC.....1000mW

Package Derating:
16-pin Plastic DIP
$ø_{JA}$.....62 °C/W
16-pin Plastic SOIC
$ø_{JA}$.....62 °C/W

## SP782 SPECIFICATIONS

Typical @ 25°C and $V_{CC} = V_{CC} \pm 5\%$ unless otherwise noted.

| | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | **CHARGE PUMP CAPACITORS: 1µF** |
| $I_{CC}$ | | 3 | 8 | mA | $V_{CC}$ = +5V, $R_L = \infty$, $V_O = 2xV_{CC}$ |
| | | 1 | 2 | mA | $V_{CC}$ = +5V, $R_L = \infty$, $V_O = V_{CC}$ |
| Shutdown $I_{CC}$ | | 10 | 25 | µA | $V_{CC}$ = +5V, SD = $V_{CC}$ |
| **POSITIVE CHARGE PUMP OUTPUT** | | | | | **CHARGE PUMP CAPACITORS: 1µF** |
| $V_{DD}$ ($2xV_{CC}$ Output) | +9.5 | +9.8 | +10.0 | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L = \infty$ |
| | +8.0 | +8.5 | | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L$ = 1kΩ |
| $V_{DD}$ ($V_{CC}$ Output) | +4.2 | +4.5 | +5.0 | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L = \infty$ |
| | +4.2 | +4.5 | | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L$ = 1kΩ |
| **NEGATIVE CHARGE PUMP OUTPUT** | | | | | **CHARGE PUMP CAPACITORS: 1µF** |
| $V_{SS}$ ($2xV_{CC}$ Output) | –9.5 | –9.8 | –10.0 | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L = \infty$ |
| | –8.0 | –8.5 | | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L$ = 1kΩ |
| $V_{SS}$ ($–V_{CC}$ Output) | –4.2 | –4.5 | –5.0 | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L = \infty$ |
| | –4.0 | –4.2 | | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L$ = 1kΩ |
| **OSCILLATOR FREQUENCY** | | | | | |
| $f_{OSC}$ | | 300 | | kHz | SD = 0V |
| **VOLTAGE CONVERSION EFFICIENCY** | | | | | |
| $V_{DD}$ (2X $V_{CC}$ Output) | 95 | 98 | | % | $R_L = \infty$ |
| $V_{DD}$ (2X $V_{CC}$ Output) | 80 | 85 | | % | $R_L$ = 1kΩ |
| $V_{SS}$ (2X $V_{CC}$ Output) | 85 | 90 | | % | $R_L = \infty$ |
| $V_{SS}$ (2X $V_{CC}$ Output) | 80 | 85 | | % | $R_L$ = 1kΩ |
| **POWER REQUIREMENTS** | | | | | |
| $V_{CC}$ | +4.75 | | +5.25 | Volts | |
| **ENVIRONMENTAL AND MECHANICAL** | | | | | |
| Operating Temperature Range | 0 | | +70 | °C | |
| Storage Temperature Range | –65 | | +150 | °C | |

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$.....+7V
$V_{DD}$.....+11V
$V_{SS}$.....–11V
Storage Temperature.....-65˚C to +150˚C
Power Dissipation
16-pin Plastic DIP.....1000mW
16-pin Plastic SOIC.....1000mW

Package Derating:
16-pin Plastic DIP
$ø_{JA}$.....62 °C/W
16-pin Plastic SOIC
$ø_{JA}$.....62 °C/W

## SP784 SPECIFICATIONS

Typical @ 25°C and $V_{CC} = V_{CC} \pm 5\%$ unless otherwise noted.

| | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | **CHARGE PUMP CAPACITORS: 10µF** |
| $I_{CC}$ | | 5 | 10 | mA | $V_{CC}$ = +5V, $R_L = \infty$, $V_O = 2xV_{CC}$ |
| | | 1 | 5 | mA | $V_{CC}$ = +5V, $R_L = \infty$, $V_O = V_{CC}$ |
| Shutdown $I_{CC}$ | | 10 | 25 | µA | $V_{CC}$ = +5V, $\overline{SD} = V_{CC}$ |
| **POSITIVE CHARGE PUMP OUTPUT** | | | | | **CHARGE PUMP CAPACITORS: 10µF** |
| $V_{DD}$ ($2xV_{CC}$ Output) | +9.0 | +9.8 | +10.0 | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L = \infty$ |
| | +8.0 | +9.5 | | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L$ = 1kΩ |
| $V_{DD}$ ($V_{CC}$ Output) | +4.5 | +4.8 | +5.0 | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L = \infty$ |
| | +4.2 | +4.5 | | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L$ = 1kΩ |
| **NEGATIVE CHARGE PUMP OUTPUT** | | | | | **CHARGE PUMP CAPACITORS: 10µF** |
| $V_{SS}$ ($2xV_{CC}$ Output) | –9.0 | –9.8 | –10.0 | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L = \infty$ |
| | –8.0 | –9.5 | | Volts | $V_{CC}$ = +5V, $D_0$ = 0V, $D_1$ = 0V $R_L$ = 1kΩ |
| $V_{SS}$ ($–V_{CC}$ Output) | –4.2 | –4.5 | –5.0 | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L = \infty$ |
| | –4.0 | –4.2 | | Volts | $V_{CC}$ = +5V, $D_0 = V_{CC}$, $D_1 = V_{CC}$ $R_L$ = 1kΩ |
| **OSCILLATOR FREQUENCY** | | | | | |
| $f_{OSC}$ | | 300 | | kHz | SD = 0V |
| **VOLTAGE CONVERSION EFFICIENCY** | | | | | |
| $V_{DD}$ (2X $V_{CC}$ Output) | 90 | 98 | | % | $R_L = \infty$ |
| $V_{DD}$ (2X $V_{CC}$ Output) | 80 | 95 | | % | $R_L$ = 1kΩ |
| $V_{SS}$ (2X $V_{CC}$ Output) | 90 | 98 | | % | $R_L = \infty$ |
| $V_{SS}$ (2X $V_{CC}$ Output) | 80 | 95 | | % | $R_L$ = 1kΩ |
| **POWER REQUIREMENTS** | | | | | |
| $V_{CC}$ | +4.75 | | +5.25 | Volts | |
| **ENVIRONMENTAL AND MECHANICAL** | | | | | |
| Operating Temperature Range | 0 | | +70 | °C | |
| Storage Temperature Range | –65 | | +150 | °C | |

## AC CHARACTERISTICS*

(Typical @ 25°C and nominal supply voltages unless otherwise noted)

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **SP782 POWER-UP DELAY TIME** | | | | | |
| **±10V OUTPUT** | | | | | |
| $t_{DVDD}$; $V_{DD}$ Power On Delay | | 1000 | | µs | $R_L$ = 1kΩ |
| $t_{DVSS}$; $V_{SS}$ Power-On Delay | | 1000 | | µs | $R_L$ = 1kΩ |
| **±5V OUTPUT** | | | | | |
| $t_{DVDD}$; $V_{DD}$ Power On Delay | | 10 | | µs | $R_L$ = 1kΩ |
| $t_{DVSS}$; $V_{SS}$ Power-On Delay | | 150 | | µs | $R_L$ = 1kΩ |
| **SP782 OUTPUT DELAY TIME** | | | | | |
| $t_{SD1}$; Switching Delay from ±10V to ±5V | | 1000 | | µs | $R_L$ = 1kΩ |
| $t_{SD2}$; Switching Delay from ±5V to ±10V | | 500 | | µs | $R_L$ = 1kΩ |
| **SP784 POWER-UP DELAY TIME** | | | | | |
| **±10V OUTPUT** | | | | | |
| $t_{DVDD}$; $V_{DD}$ Power On Delay | | 5 | | ms | $R_L$ = 1kΩ |
| $t_{DVSS}$; $V_{SS}$ Power-On Delay | | 5 | | ms | $R_L$ = 1kΩ |
| **±5V OUTPUT** | | | | | |
| $t_{DVDD}$; $V_{DD}$ Power On Delay | | 10 | | µs | $R_L$ = 1kΩ |
| $t_{DVSS}$; $V_{SS}$ Power-On Delay | | 1000 | | µs | $R_L$ = 1kΩ |
| **SP784 OUTPUT DELAY TIME** | | | | | |
| $t_{SD1}$; Switching Delay from ±10V to ±5V | | 10 | | ms | $R_L$ = 1kΩ |
| $t_{SD2}$; Switching Delay from ±5V to ±10V | | 2 | | ms | $R_L$ = 1kΩ |

* - Using the charge pump capacitor values specified in the previous pages for each device.

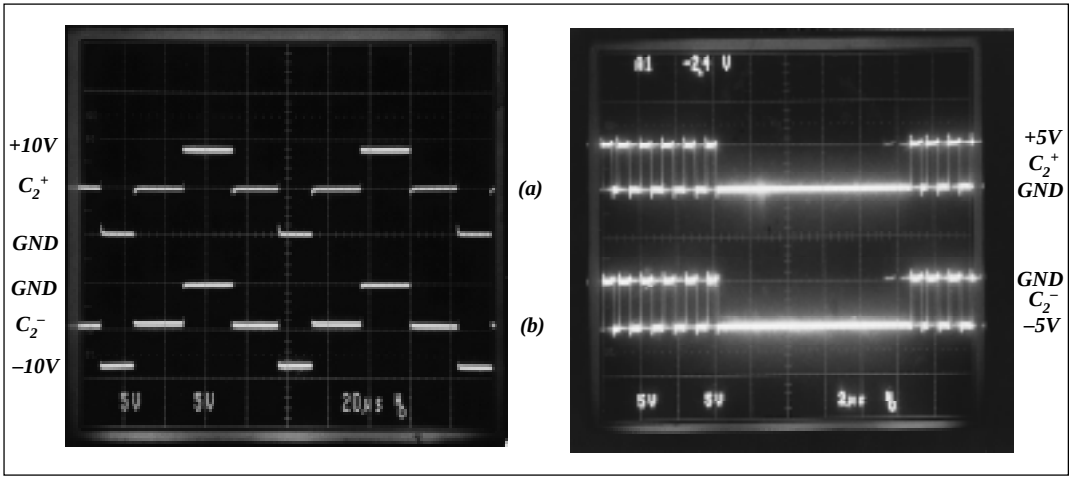
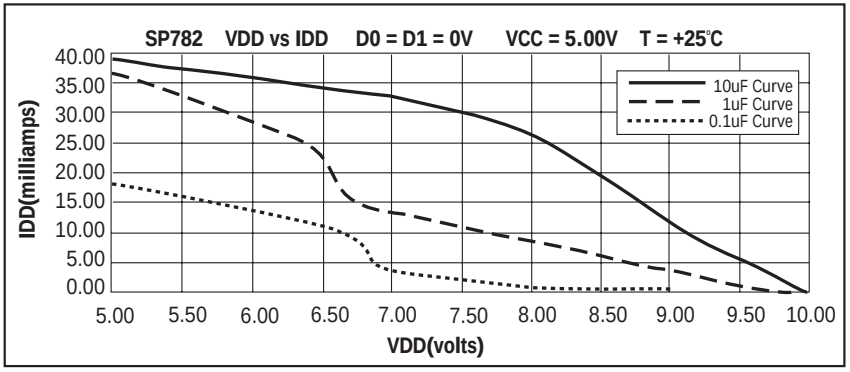
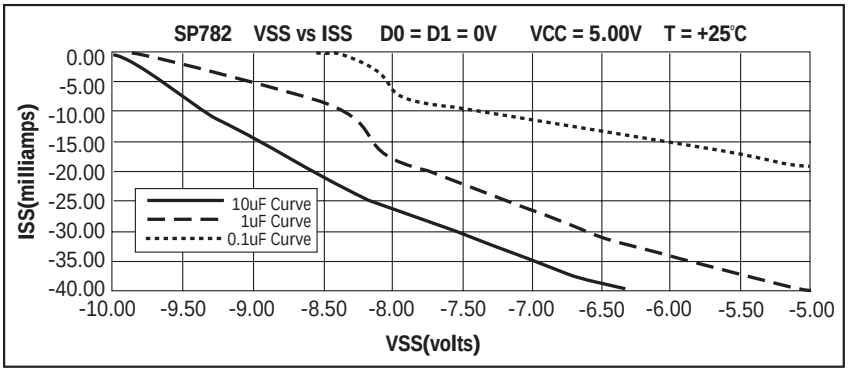
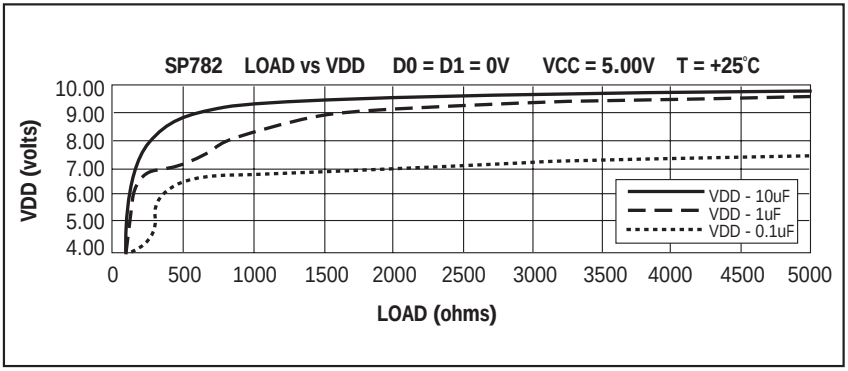


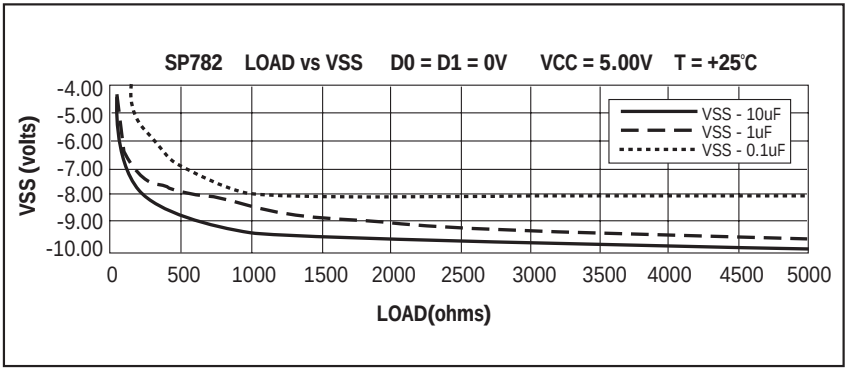

*Figure 1. Charge Pump Waveforms*

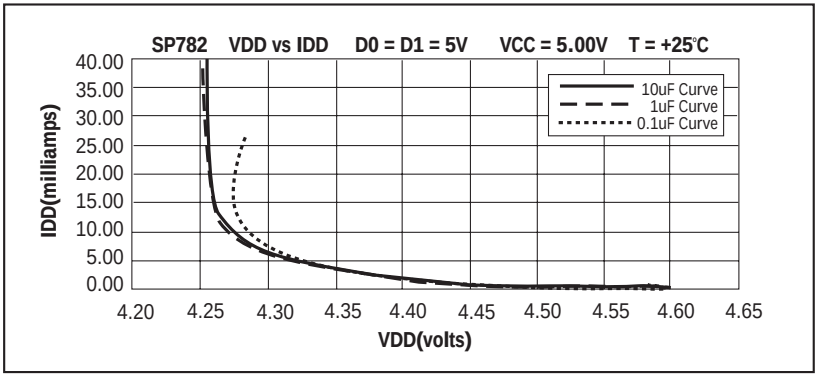


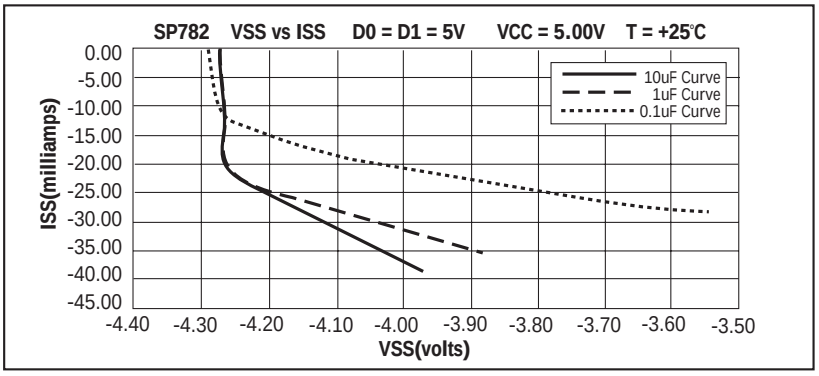



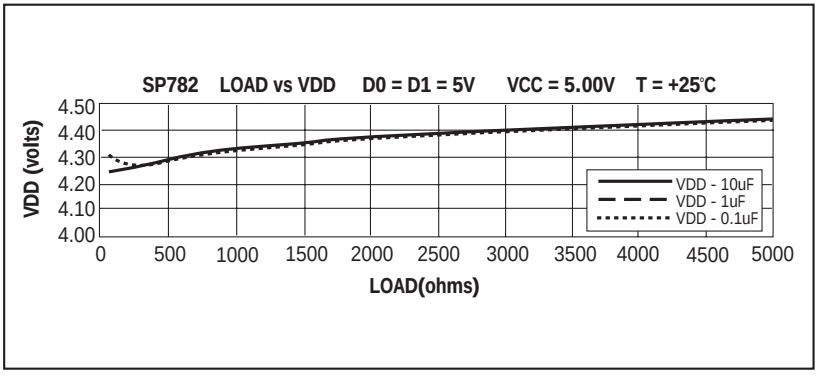



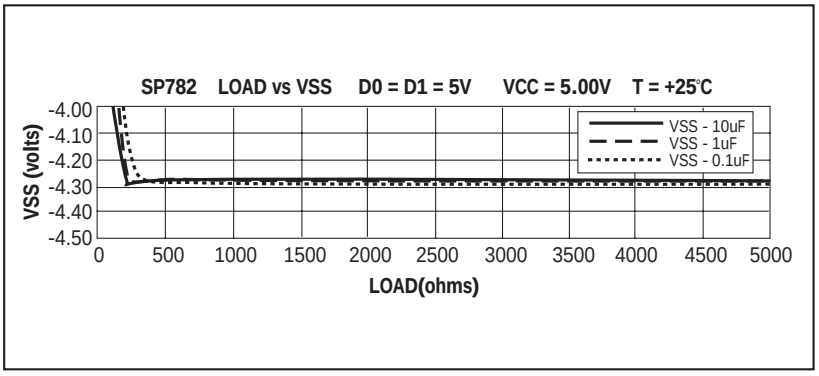



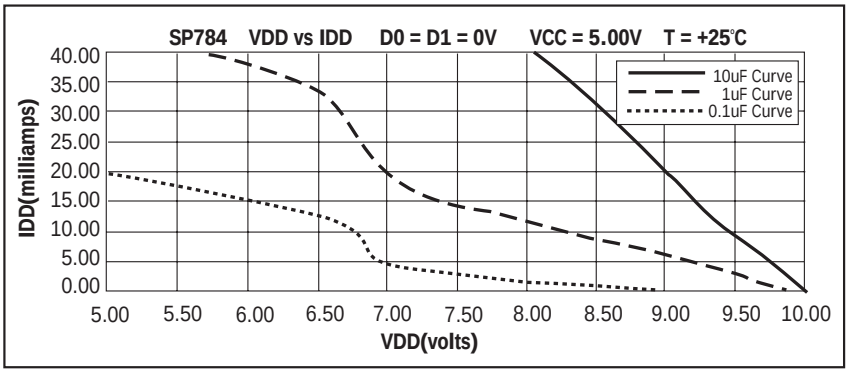


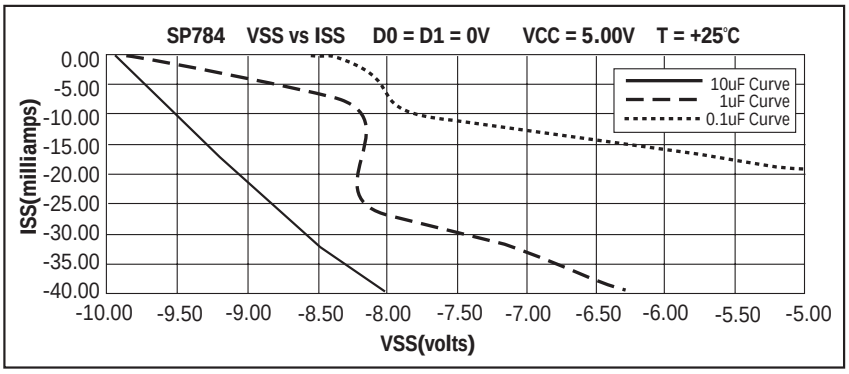



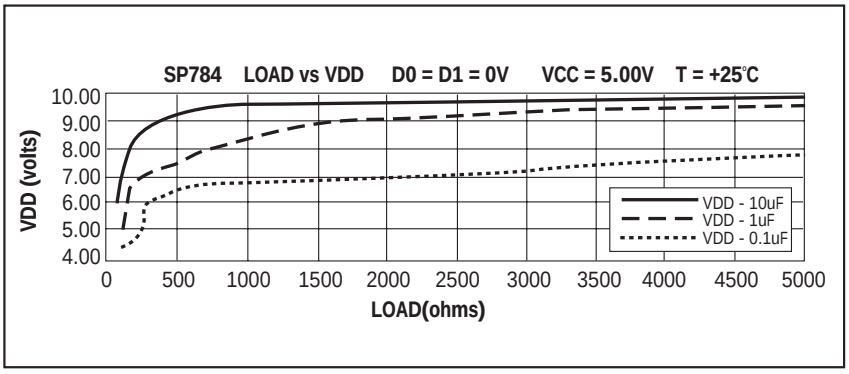



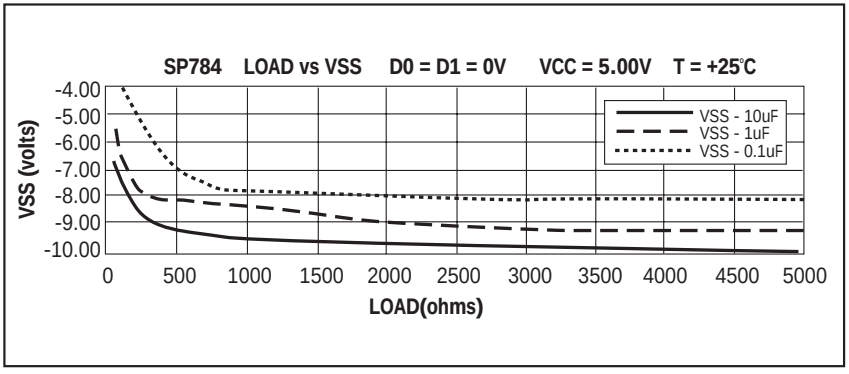



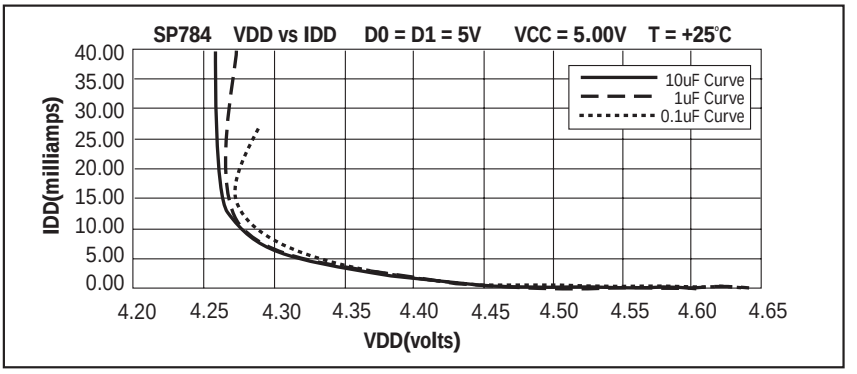


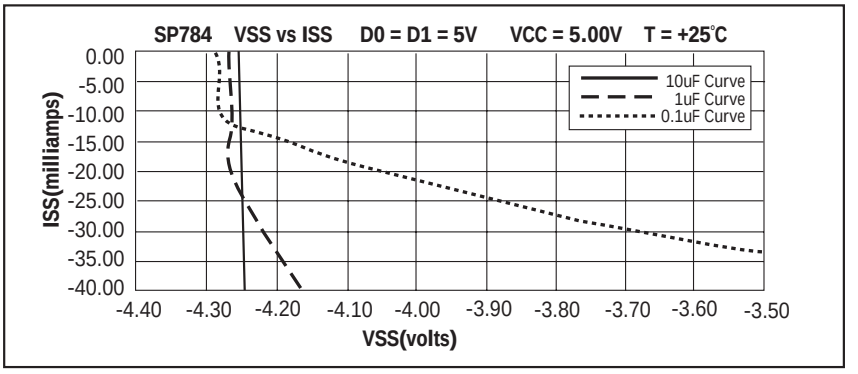



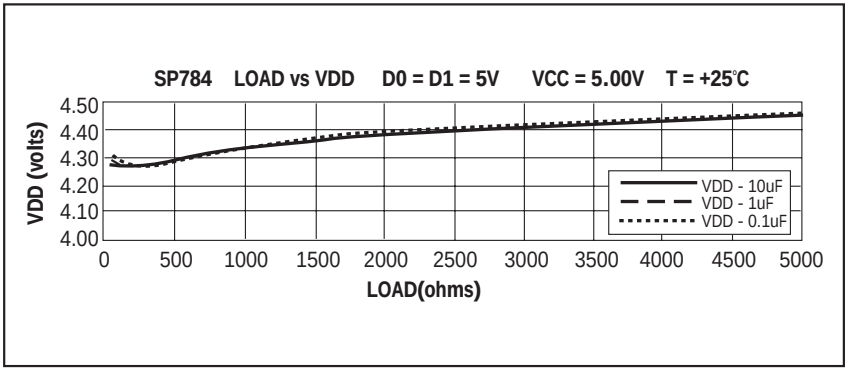



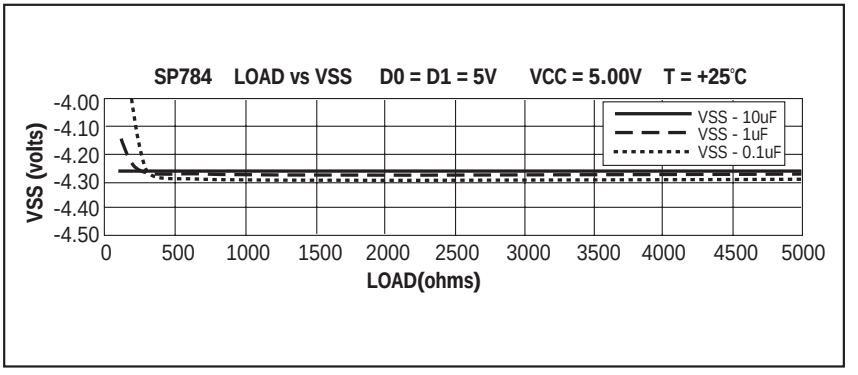





## THEORY OF OPERATION

The **SP782/784's** charge pump design is based on **Sipex's** original patented charge pump design (5,306,954) which uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. In addition, the **SP782/784** charge pump incorporates a "programmable" feature that produces an output of ±10V or ±5V for $V_{SS}$ and $V_{DD}$ by two control pins, D0 and D1. The charge pump requires external capacitors to store the charge. Figure 1 shows the waveform found on the positive and negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1 (±10V)

— $V_{SS}$ charge storage — During this phase of the clock cycle, the positive side of capacitors $C_1$ and $C_2$ are initially charged to +5V. $C_1^+$ is then switched to ground and the charge on $C_1^-$ is transferred to $C_2^-$. Since $C_2^+$ is connected to +5V, the voltage potential across capacitor $C_2$ is now 10V.

### Phase 1 (±5V)

— $V_{SS}$ & $V_{DD}$ charge storage and transfer — With the $C_1$ and $C_2$ capacitors initially charged to +5V, $C_1^+$ is then switched to ground and the charge on $C_1^-$ is transferred to the $V_{SS}$ storage capacitor. Simultaneously the $C_2^-$ is switched to ground and 5V charge on $C_2^+$ is transferred to the $V_{DD}$ storage capacitor.

### Phase 2 (±10V)

— $V_{SS}$ transfer — Phase two of the clock connects the negative terminal of $C_2$ to the $V_{SS}$ storage capacitor and the positive terminal of $C_2$ to ground, and transfers the generated –l0V or the generated –5V to $C_3$. Simultaneously, the positive side of capacitor $C_1$ is switched to +5V and the negative side is connected to ground.

### Phase 2 (±5V)

— $V_{SS}$ & $V_{DD}$ charge storage — $C_1^+$ is reconnected to $V_{CC}$ to recharge the $C_1$ capacitor. $C_2^+$ is switched to ground and $C_2^-$ is connected to $C_3$. The 5V charge from Phase 1 is now transferred to the $V_{SS}$ storage capacitor. $V_{SS}$ receives a continuous charge from either $C_1$ or $C_2$. With the C1 capacitor charged to 5V, the cycle begins again.

### Phase 3

— $V_{DD}$ charge storage — The third phase of the clock is identical to the first phase — the charge transferred in $C_1$ produces –5V in the negative terminal of $C_1$, which is applied to the negative side of capacitor $C_2$. Since $C_2^+$ is at +5V, the voltage potential across $C_2$ is l0V. For the 5V output, $C_2^+$ is connected to ground so that the potential on $C_2$ is only +5V.

### Phase 4

— $V_{DD}$ transfer — The fourth phase of the clock connects the negative terminal of $C_2$ to ground and transfers the generated l0V or the generated 5V across $C_2$ to $C_4$, the $V_{DD}$ storage capacitor. Again, simultaneously with this, the positive side of capacitor $C_1$ is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both $V_{DD}$ and $V_{SS}$ are separately generated from $V_{CC}$ in a no–load condition, $V_{DD}$ and $V_{SS}$ will be symmetrical. Older charge pump approaches that generate $V^-$ from $V^+$ will show a decrease in the magnitude of $V^-$ compared to $V^+$ due to the inherent inefficiencies in the design.

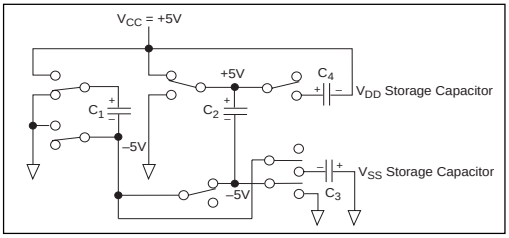



***Figure 2. Charge Pump Phase 1 for ±10V.***

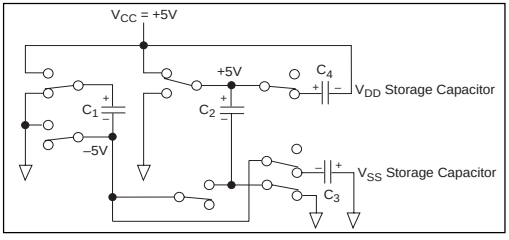



***Figure 3. Charge Pump Phase 1 for ±5V.***

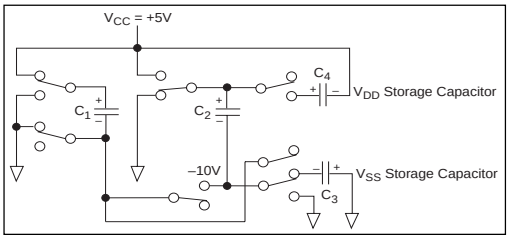



*Figure 4. Charge Pump Phase 2 for ±10V.*

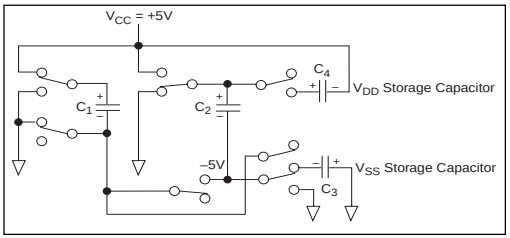



*Figure 5. Charge Pump Phase 2 for ±5V.*

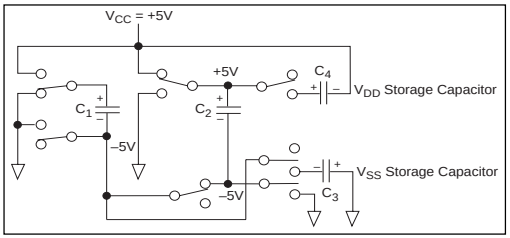



*Figure 6. Charge Pump Phase 3.*

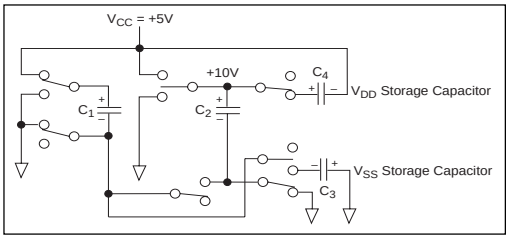



*Figure 7. Charge Pump Phase 4.*

The oscillator frequency or clock rate for the charge pump is designed for low power operation. The oscillator changes from a high frequency mode (400kHz) to a low frequency mode (20kHz) when the SD pin goes to a logic "1". The lower frequency allows the **SP782/ SP784** to conserve power when the outputs are not being used.

## EFFICIENCY INFORMATION

A charge pump theoretically produces a doubled voltage at 100% efficiency. However in the real world, there is a small voltage drop on the output which reduces the output efficiency. The **SP782** and **SP784** can usually run 99.9% efficient without driving a load. While driving a 1kΩ load, the **SP782** and **SP784** remain at least 90% efficient.

Total Output Voltage Efficiency =
$[(V_{OUT}+) / (2*V_{CC})] + [(V_{OUT}–) / (–2*V_{CC})]$ ;

$V_{OUT}+ = 2*V_{CC} + V_{DROP}+$

$V_{OUT}– = –2*V_{CC} + V_{DROP}–$

$V_{DROP}– = (I–)*(R_{OUT}–)$

$V_{DROP}+ = (I+)*(R_{OUT}+)$

Power Loss = $I_{OUT}*(V_{DROP})$

The efficiency changes as the external charge pump capacitors are varied. Larger capacitor values will strengthen the output and reduce output ripple usually found in all charge pumps. Although smaller capacitors will cost less and save board space, lower values will reduce the output drive capability.

The output voltage ripple is also affected by the capacitors, specifically C3 and C4. Larger values will reduce the output ripple for a given load of current. The current drawn from either output is supplied by just the storage capacitor, C3 or C4, during one half cycle of the internal oscillator. Note that the output current from the postive charge pump is the load current plus the current taken by the negative charge pump. Thus the formula representation for the output ripple voltage is:

$V_{RIPPLE}+ = \{1 / (f_{OSC}) * 1 / C3\} * 0.5 * I_{OUT}+$

$V_{RIPPLE}– = \{1 / (f_{OSC}) * 1 / C3\} * 0.5 * I_{OUT}–$

To minimize the output ripple, the C3 and C4 storage capacitors can be increased to over 10µF whereas the pump capacitors can range from 1µF to 5µF.

Multiple **SP782/784** charge pumps can be connected in parallel. However, the output resistance on both pump outputs will be reduced. The effective output resistance is the output resistance of one pump divided by the number of charge pumps connected. It is important to keep the C1 and C2 capacitors separate for each charge pump. The storage capacitors, C3 and C4, can be shared.

## SHUTDOWN MODE

The internal oscillator of the **SP782** and **SP784** can be shutdown through the SD pin. In this state, the $V_{DD}$ and $V_{SS}$ outputs are inactive and the power supply current reduces to 10µA.

## LATCH ENABLE PIN

The **SP782** and **SP784** includes a control pin (LAT) that latches the D0 and D1 control lines. Connecting this pin to a logic HIGH state will allow transparent operation of the D0 and D1 control lines. This input can be left floating since there is an internal pull-up resistor which will allow the latch to be transparent.

## APPLICATIONS INFORMATION

The **SP782** and **SP784** can be used in various applications where ±10V is needed from a +5V source. Analog switches, op-amp power supplies, and LCD biasing are some applications where the charge pumps can be used.

The charge pump can also be used for supplying voltage rails for RS-232 drivers needing ±12V. The ±10V output from the charge pump is more than adequate to provide the proper $V_{OH}$ and $V_{OL}$ levels at the driver output.

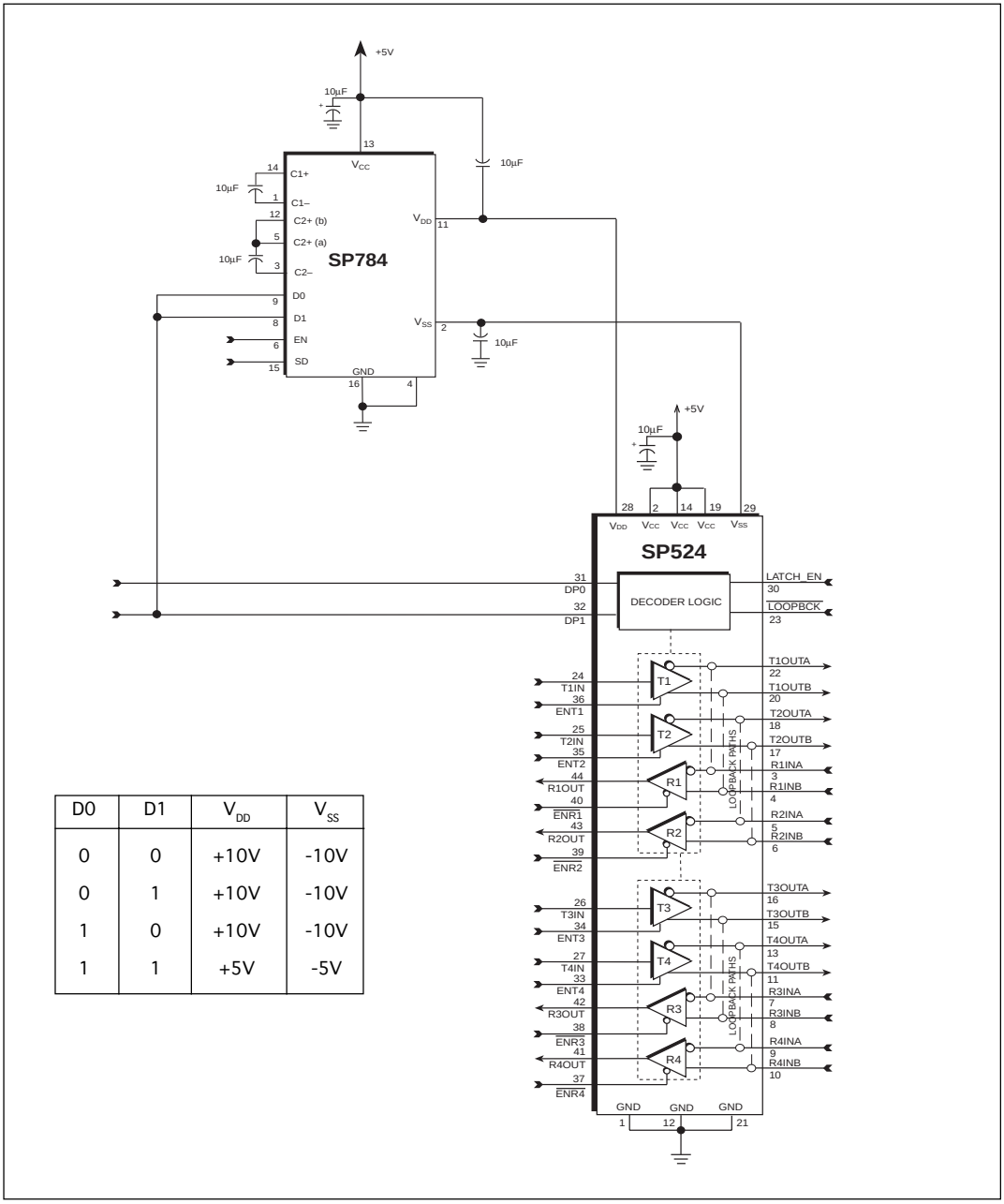
Figure 8 shows how the **SP784** can be used in conjunction with the SP524 multiprotocol transceiver IC. The programmability is ideal for RS-232 and RS-423 levels. The RS-232 driver output voltage swing ranges from ±5V to ±15V. In order to meet this requirement, the charge pump must generate ±10V to the transceiver IC.

The RS-423 driver output voltage range is ±4.0V to ±6.0V. When the SP524 transceiver is programmed to RS-423 mode (V.10), the charge pump now provides ±5V, through D0 and D1, thus allowing the driver outputs to comply with $V_{OC} \leq 6.0V$ as well as the $V_T$ requirement of ±4.0V minimum with a 450Ω load to ground.

In older configurations, separate DC sources needed to be configured or regulated down from ±10V to ±5V in a given application. A typical charge pump providing $V_{DD}$ and $V_{SS}$ would require external clamping such as 5V Zener diodes. RS-423 (V.10) is usually found in RS-449, EIA-530, EIA-530A, and V.36 modes.

When the control lines D0 and D1 are both at a logic HIGH, $V_{DD}$ = +5V and $V_{SS}$ = -5V. All other inputs to the control lines result in $V_{DD}$ = +10V and $V_{SS}$ = -10V. Control of the **SP784** in an application with **Sipex's SP524** can be found in *Figure 8*.




| D0 | D1 | $V_{DD}$ | $V_{SS}$ |
|---|---|---|---|
| 0 | 0 | +10V | -10V |
| 0 | 1 | +10V | -10V |
| 1 | 0 | +10V | -10V |
| 1 | 1 | +5V | -5V |

***Figure 8. SP784 Application w/ SP524 Multi-Protocol Transceiver IC.***

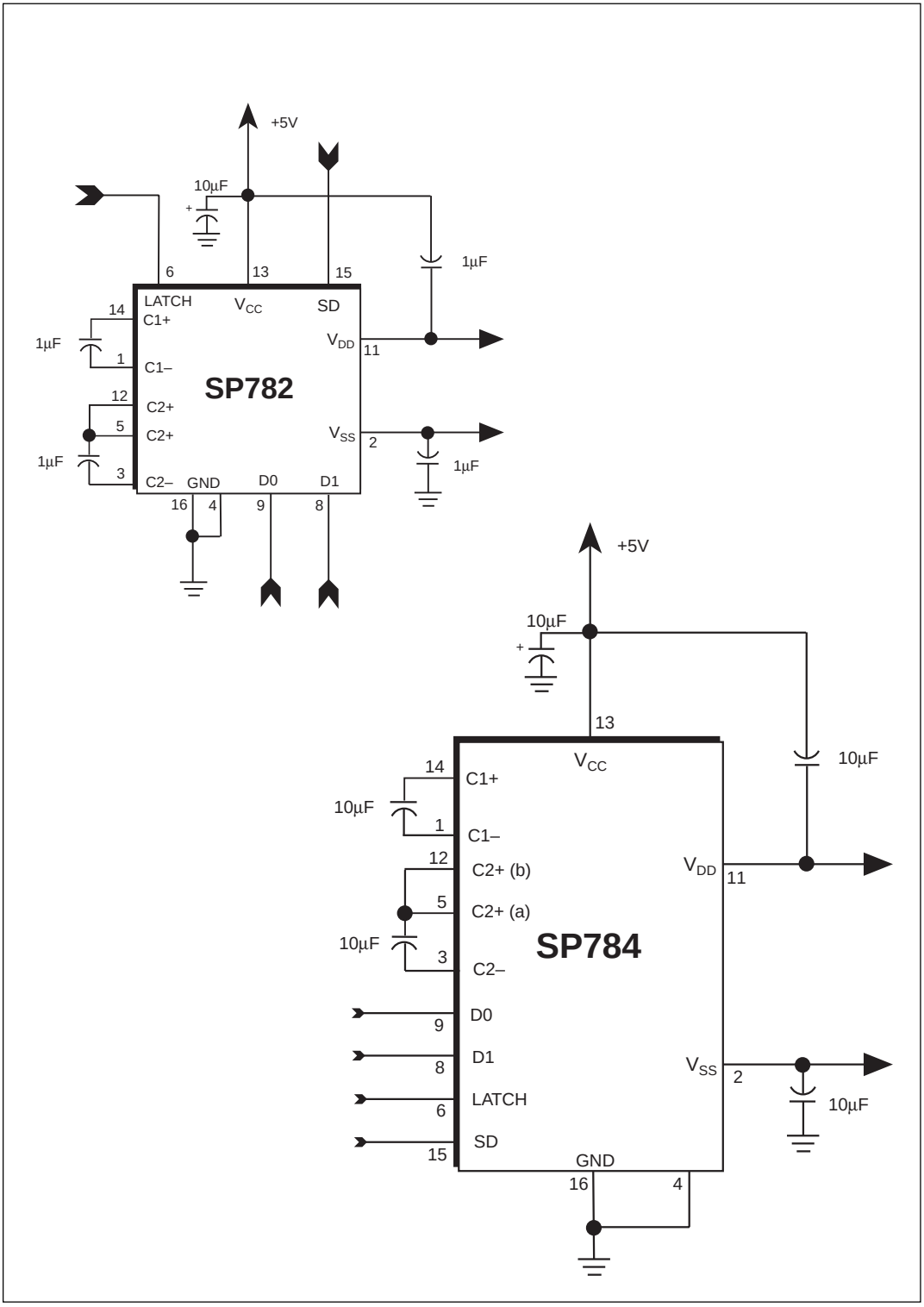
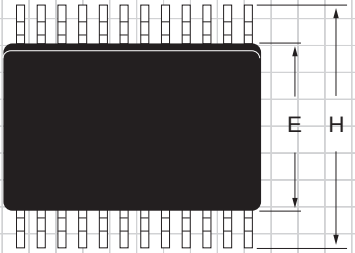
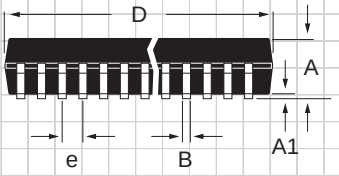


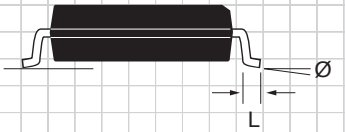

***Figure 9. SP782 and SP784 Block Diagrams***

## PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)



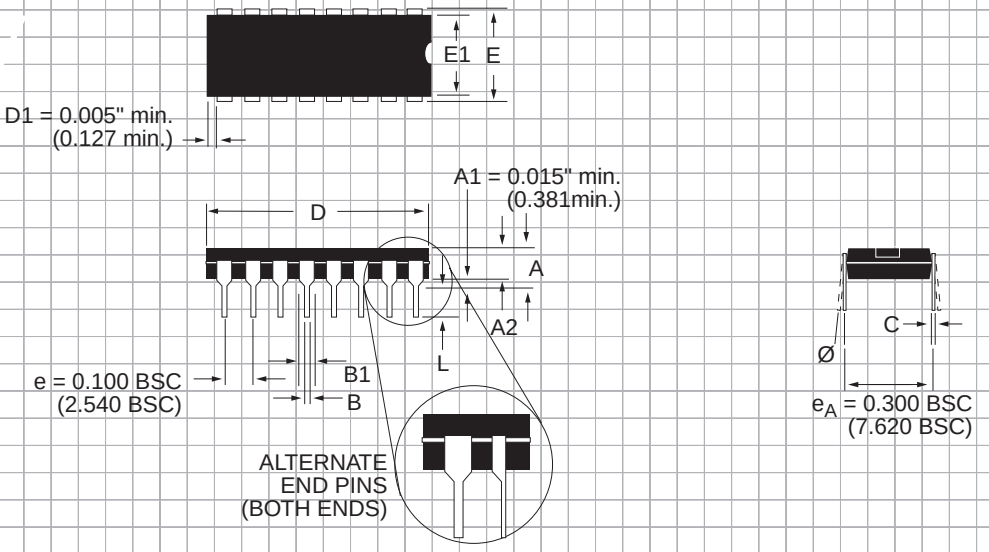




| DIMENSIONS (Inches) Minimum/Maximum (mm) | 16–PIN |
|---|---|
| A | 0.093/0.104 (2.352/2.649) |
| A1 | 0.004/0.012 (0.102/0.300) |
| B | 0.013/0.020 (0.330/0.508) |
| D | 0.398/0.406 (10.11/10.31) |
| E | 0.291/0.299 (7.402/7.600) |
| e | 0.050 BSC (1.270 BSC) |
| H | 0.394/0.419 (10.00/10.64) |
| L | 0.016/0.050 (0.406/1.270) |
| Ø | 0°/8° (0°/8°) |

## PACKAGE: 16-PIN PLASTIC DUAL–IN–LINE (NARROW)




| DIMENSIONS (Inches) Minimum/Maximum (mm) | 16–PIN |
|---|---|
| A | –/0.210 (–/5.334) |
| A2 | 0.115/0.195 (2.921/4.953) |
| B | 0.014/0.022 (0.356/0.559) |
| B1 | 0.045/0.070 (1.143/1.778) |
| C | 0.008/0.014 (0.203/0.356) |
| D | 0.780/0.800 (19.812/20.320) |
| E | 0.300/0.325 (7.620/8.255) |
| E1 | 0.240/0.280 (6.096/7.112) |
| L | 0.115/0.150 (2.921/3.810) |
| Ø | 0°/ 15° (0°/15°) |

## ORDERING INFORMATION

| Model | Temperature Range | Package Types |
|---|---|---|
| **SP782CP** | 0°C to +70°C | 16-pin Plastic DIP |
| **SP784CP** | 0°C to +70°C | 16-pin Plastic DIP |
| **SP782CT** | 0°C to +70°C | 16-pin SOIC |
| **SP784CT** | 0°C to +70°C | 16-pin SOIC |

Please consult the factory for pricing and availability on a Tape-On-Reel option.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