


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1. FUNCTIONS & FEATURES

- LCD TYPE:

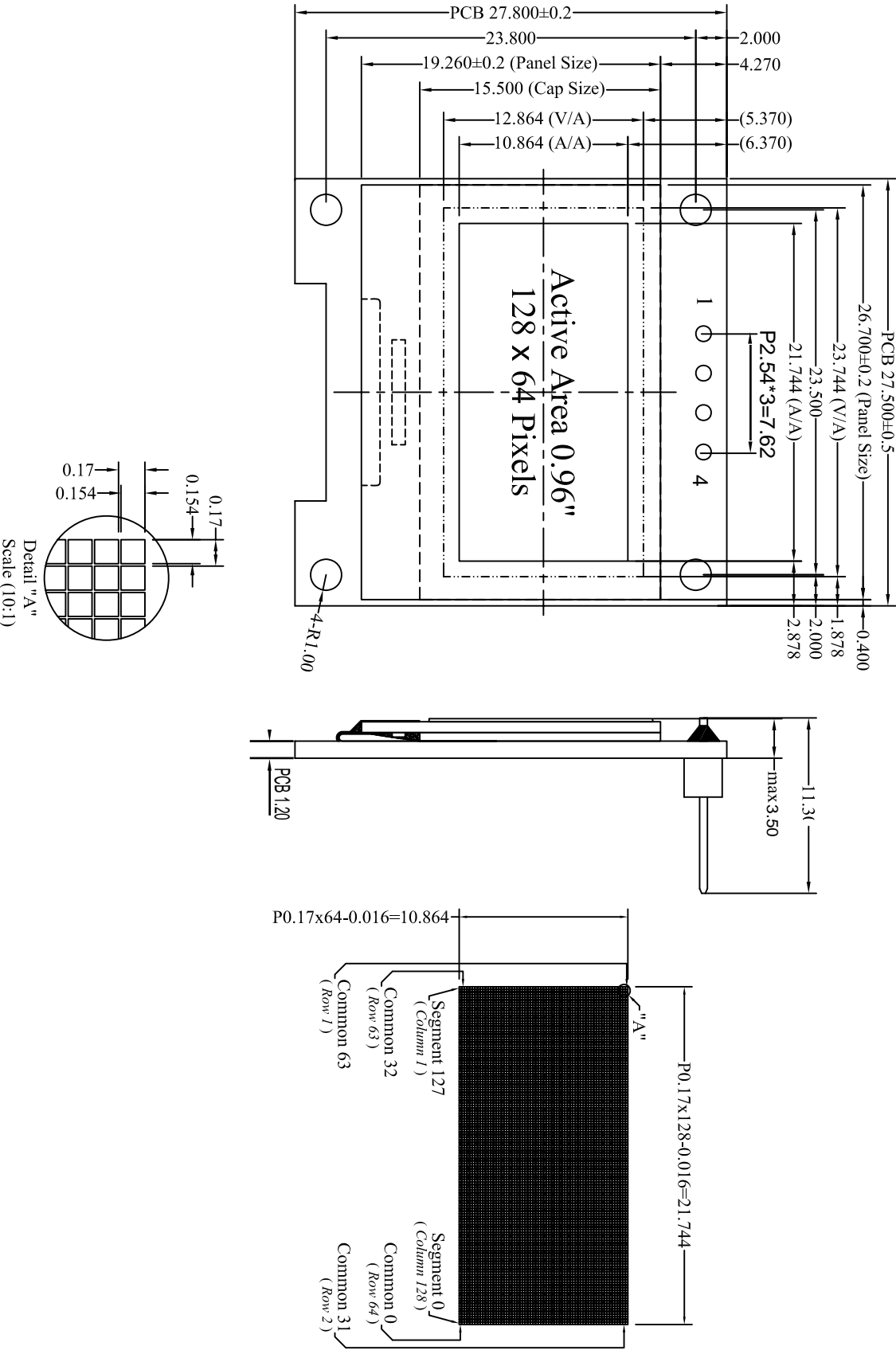
MODULE MODEL	LCD TYPE	REMARK
GME12864-11	0.96" OLED Passive Matrix White	

- Driving Scheme : 1/64 Duty,
- Viewing direction : 6 O'clock
- Drive IC : SSD1306
- Power Supply Voltage : 3.0V
- V_{CC} : 12.0V
- Interface : IIC
- RoHS Compliant

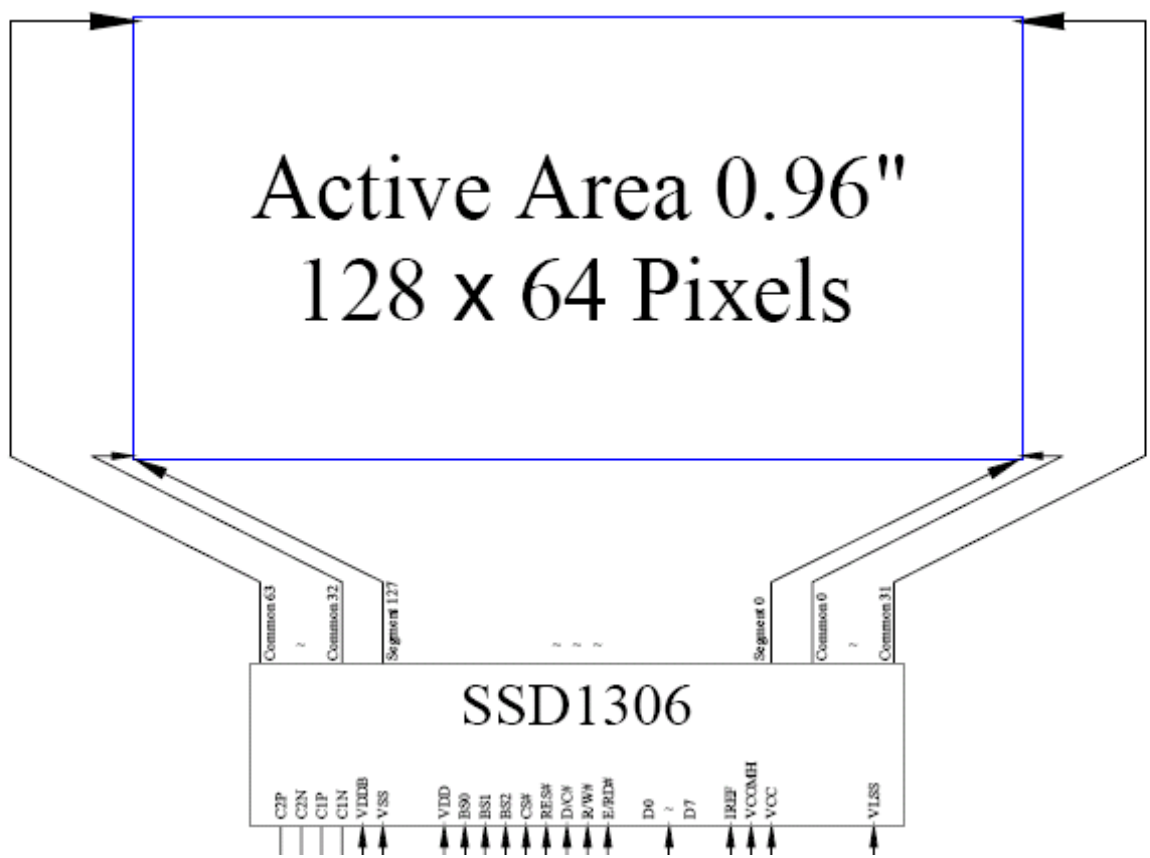
2. MECHANICAL SPECIFICATIONS

- Module Size : 27.50 (L) x 27.80 (W) x 3.50Max (T) mm
- Viewing Area : 23.744(L) x 12.864 (W) mm
- Active Area : 21.744 (L) x 10.864 (W) mm
- Dot Pitch : 0.154 (W) x 0.154 (H) mm
- Dot Size : 0.17(W) x 0.17(H) mm

3. EXTERNAL DIMENSIONS ( unit: mm)



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

PIN	SYMBOL	Descriptions
1	GND	Ground of Logic Circuit
2	VDD	Power Supply for Logic
3	SCK	Serial clock input.
4	SDA	Serial data input.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V _{CC}	0	16	V	1, 2
<i>Supply Voltage for DC/DC</i>	<i>V_{BAT}</i>	<i>-0.3</i>	<i>5</i>	<i>V</i>	<i>1, 2</i>
Operating Temperature	T _{OP}	-40	85	°C	
Storage Temperature	T _{STG}	-40	85	°C	3
Life Time (120 cd/m ²)		10,000	-	hour	4
Life Time (80 cd/m ²)		30,000	-	hour	4
Life Time (60 cd/m ²)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

7. ELECTRICAL CHARACTERISTICS

7.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V _{CC} Supplied Externally)	L _{br}	Note 5	80	100	-	cd/m ²
<i>Brightness (V_{CC} Generated by Internal DC/DC)</i>	<i>L_{br}</i>	<i>Note 6</i>	<i>50</i>	<i>60</i>	<i>-</i>	<i>cd/m²</i>
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.20	0.14 0.24	0.18 0.28	
C.I.E. (Yellow)	(x) (y)	C.I.E. 1931	0.43 0.45	0.47 0.49	0.51 0.53	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V & 7.25V.

Software configuration follows Section 4.4 Initialization.

7.2. DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	11.5	12.0	12.5	V
Supply Voltage for DC/DC	V_{SAT}	Internal DC/DC Enable	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	Note 6 (Internal DC/DC Enable)	7.0	-	7.5	V
High Level Input	V_{IH}	$I_{OUT} = 100\mu A, 3.3MHz$	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}	$I_{OUT} = 100\mu A, 3.3MHz$	$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.1 \times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	12.3	16	mA
Operating Current for V_{SAT} (V_{CC} Generated by Internal DC/DC)	I_{SAT}	Note 8	-	21	28.0	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5 & 6: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: $V_{DD} = 2.8V, V_{CC} = 12V, 100\%$ Display Area Turn on.

Note 8: $V_{DD} = 2.8V, V_{CC} = 7.25V, 100\%$ Display Area Turn on.

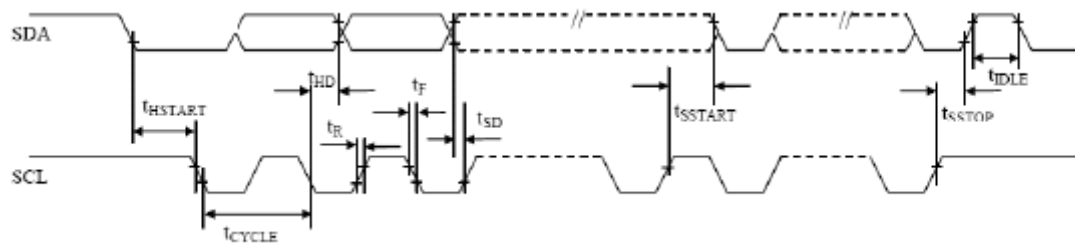
* Software configuration follows Section 4.4 Initialization.

7.3.AC CHARACTERISTICS

1 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA _{OUT} " Pin)	0	-	ns
	Data Hold Time (for "SDA _{IN} " Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_{R}	Rise Time for Data and Clock Pin		300	ns
t_{F}	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



8. COMMANDS

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81	1	0	0	0	0	0	0	1	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	A4/A5	1	0	1	0	0	1	0	X ₀	Entire Display ON	A4h, X ₀ =0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X ₀ =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X ₀	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode

2. Scrolling Command Table																				
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description									
0	26/27	0	0	1	0	0	1	1	X ₀	Continuous	26h, X[0]=0, Right Horizontal Scroll									
0	A[7:0]	0	0	0	0	0	0	0	0	Horizontal Scroll	27h, X[0]=1, Left Horizontal Scroll									
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀	Setup	(Horizontal scroll by 1 column)									
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀		A[7:0] : Dummy byte (Set as 00h)									
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀		B[2:0] : Define start page address									
0	E[7:0]	0	0	0	0	0	0	0	0		<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
0	F[7:0]	1	1	1	1	1	1	1	1		<table><tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr><tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr></table>	000b – 5 frames	100b – 3 frames	001b – 64 frames	101b – 4 frames	010b – 128 frames	110b – 25 frame	011b – 256 frames	111b – 2 frame	
000b – 5 frames	100b – 3 frames																			
001b – 64 frames	101b – 4 frames																			
010b – 128 frames	110b – 25 frame																			
011b – 256 frames	111b – 2 frame																			
											C[2:0] : Set time interval between each scroll step in terms of frame frequency									
											<table><tr><td>000b – 5 frames</td><td>100b – 3 frames</td></tr><tr><td>001b – 64 frames</td><td>101b – 4 frames</td></tr><tr><td>010b – 128 frames</td><td>110b – 25 frame</td></tr><tr><td>011b – 256 frames</td><td>111b – 2 frame</td></tr></table>	000b – 5 frames	100b – 3 frames	001b – 64 frames	101b – 4 frames	010b – 128 frames	110b – 25 frame	011b – 256 frames	111b – 2 frame	
000b – 5 frames	100b – 3 frames																			
001b – 64 frames	101b – 4 frames																			
010b – 128 frames	110b – 25 frame																			
011b – 256 frames	111b – 2 frame																			
											D[2:0] : Define end page address									
											<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
											The value of D[2:0] must be larger or equal to B[2:0]									
											E[7:0] : Dummy byte (Set as 00h)									
											F[7:0] : Dummy byte (Set as FFh)									

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X ₁	X ₀	Continuous	29h, X ₁ X ₀ =01b : Vertical and Right Horizontal Scroll
0	A[2:0]	0	0	0	0	0	0	0	0	Vertical and	2Ah, X ₁ X ₀ =10b : Vertical and Left Horizontal Scroll
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀	Horizontal Scroll	(Horizontal scroll by 1 column)
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀	Setup	A[7:0] : Dummy byte
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀		
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		B[2:0] : Define start page address
											000b - PAGE0 011b - PAGE3 110b - PAGE6
											001b - PAGE1 100b - PAGE4 111b - PAGE7
											010b - PAGE2 101b - PAGE5
											C[2:0] : Set time interval between each scroll step in terms of frame frequency
											000b - 5 frames 100b - 3 frames
											001b - 64 frames 101b - 4 frames
											010b - 128 frames 110b - 25 frame
											011b - 256 frames 111b - 2 frame
											D[2:0] : Define end page address
											000b - PAGE0 011b - PAGE3 110b - PAGE6
											001b - PAGE1 100b - PAGE4 111b - PAGE7
											010b - PAGE2 101b - PAGE5
											The value of D[2:0] must be larger or equal to B[2:0]
											E[5:0] : Vertical scrolling offset
											e.g. E[5:0]=01h refer to offset =1 row
											E[5:0]=3Fh refer to offset =63 rows
											Note
											(1) No continuous vertical scrolling is available.
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah.
											Note
											(1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:
											Valid command sequence 1: 26h ;2Fh.
											Valid command sequence 2: 27h ;2Fh.
											Valid command sequence 3: 29h ;2Fh.
											Valid command sequence 4: 2Ah ;2Fh.
											For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

2. Scrolling Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDR4 (i.e. row 0). [RESET = 0]
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]
											Note
											(1) A[5:0]+B[6:0] <= MUX ratio
											(2) B[6:0] <= MUX ratio
											(3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0]
											(3b) Set Display Start Line (X ₀ X ₁ X ₂ X ₃ X ₄ X ₅ of 40h~7Fh) < B[6:0]
											(4) The last row of the scroll area shifts to the first row of the scroll area.
											(5) For 64d MUX display
											A[5:0] = 0, B[6:0]=64 : whole area scrolls
											A[5:0]= 0, B[6:0] < 64 : top area scrolls
											A[5:0] + B[6:0] < 64 : central area scrolls
											A[5:0] + B[6:0] = 64 : bottom area scrolls

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note ¹⁾ This command is only for page addressing mode
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note ¹⁾ This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A ₁	0 A ₀	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	0 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0] : Column end address, range : 0-127d, (RESET =127d) Note ¹⁾ This command is only for horizontal or vertical addressing mode.

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A ₂ B ₂	1 A ₁ B ₁	0 A ₀ B ₀	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) Note ¹⁾ This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X ₂	X ₁	X ₀	Set Page Start Address for Page Addressing Mode	Set GDDR4M Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. Note ¹⁾ This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₀ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0]: from 16MUX to 64MUX, RESET=111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0	D3	1	1	0	1	0	0	1	1	Set Display Offset	Set vertical shift by COM from 0d-63d The value is reset to 00h after RESET.
0	DA	1	1	0	1	1	0	1	0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4]: Set the Oscillator Frequency, F _{OSC} . Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Set Pre-charge Period	A[3:0]: Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4]: Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	DB	1	1	0	1	1	0	1	1	Set V _{COMH} Deselect Level	A[6:4] Hex code V _{COMH} deselect level 000b 00h ~ 0.65 x V _{CC} 010b 20h ~ 0.77 x V _{CC} (RESET) 011b 30h ~ 0.83 x V _{CC}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

Note

(1) “*” stands for “Don’t care”.

9. FUNCTIONAL SPECIFICATION

9.1 Commands

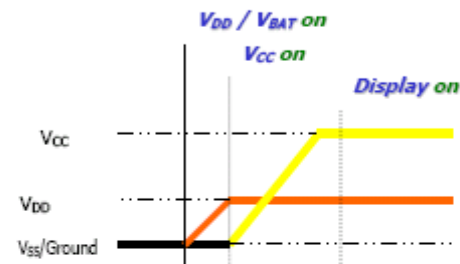
Refer to the Technical Manual for the SSD1306

9.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

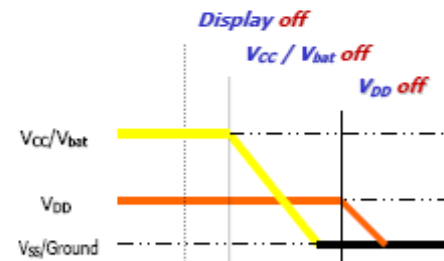
9.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/V_{BAT}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



9.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms
(When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

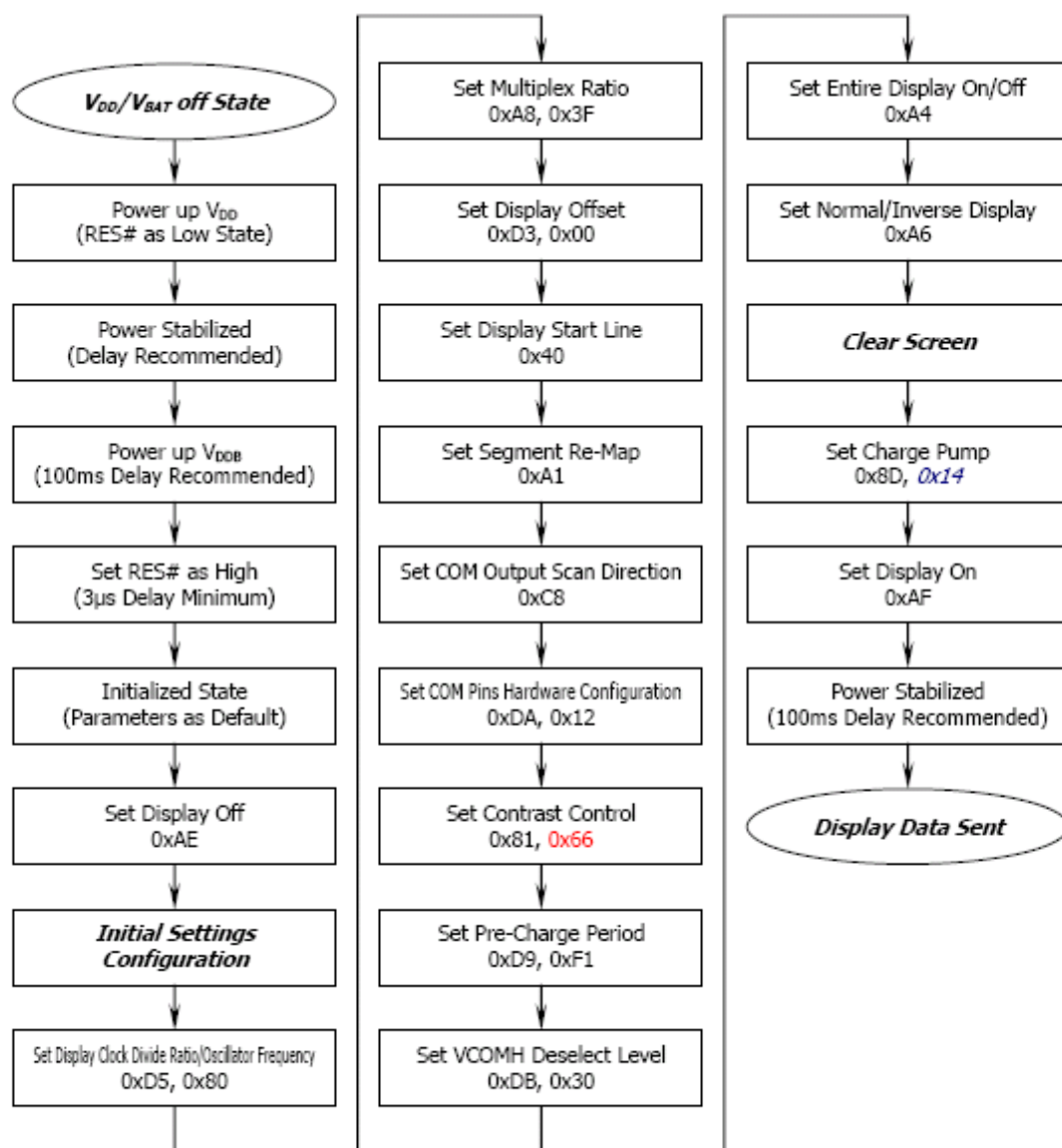
- 1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
- 2) V_{CC}/V_{BAT} should be kept float (disable) when it is OFF.
- 3) Power Pins (V_{DD} , V_{CC} , V_{BAT}) can never be pulled to ground under any circumstance.
- 4) V_{DD} should not be power down before V_{CC}/V_{BAT} power down.

9.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

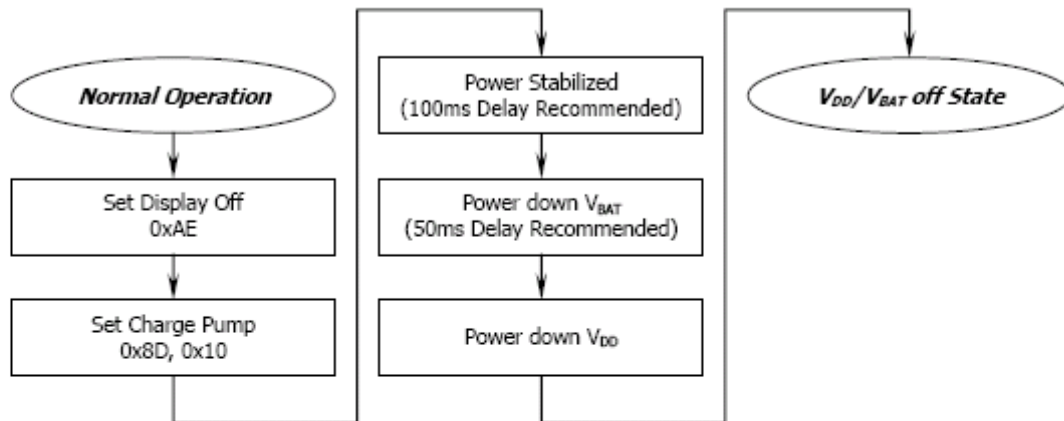
1. Display is OFF
2. 128x64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

9.4 Actual Application Example

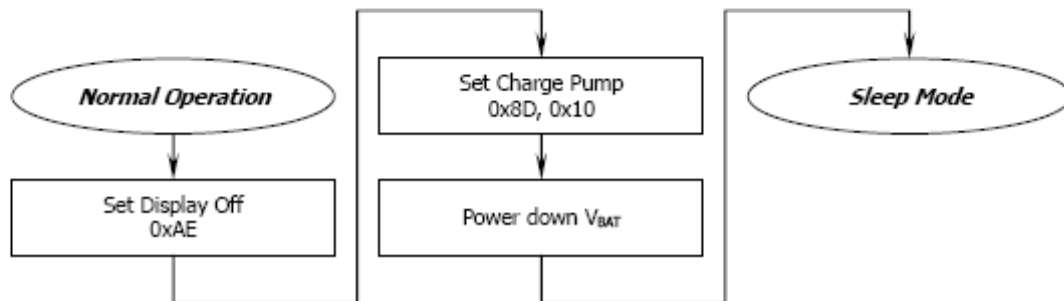


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

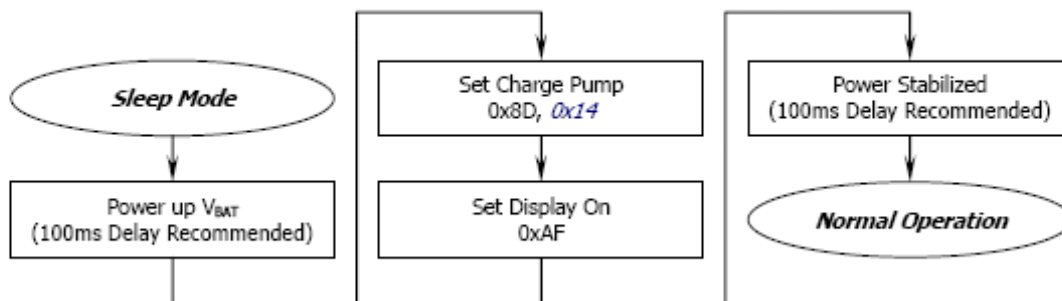
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>

**10. MODULE ACCEPT QUALITY LEVEL (AQL)**

10.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

10.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

11. RELIABILITY TEST.**11.1 Contents of Reliability Tests**

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇌ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

11.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

12. QUALITY DESCRIPTION & APPLICATION NOTE

Please refer to "General Inspection Criteria" document.