

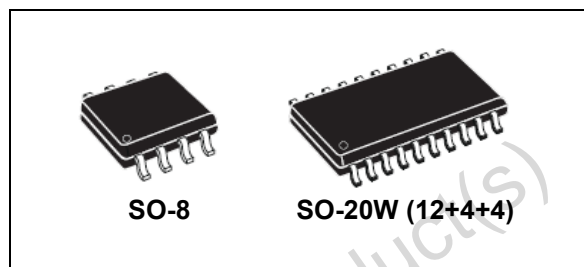


## L4949E

### Multifunction very low drop voltage regulator

#### Features

- Operating DC supply voltage range 5 V - 28 V
- Transient supply voltage up to 40V
- Extremely low quiescent current in standby mode
- High precision standby output voltage  $5V \pm 1\%$
- Output current capability up to 100mA
- Very low dropout voltage less than 0.5V
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Voltage sense comparator
- Thermal shutdown and short circuit protections



#### Description

The L4949E is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-8	L4949ED	L4949ED013TR
SO-20W	L4949EP	L4949EP013TR

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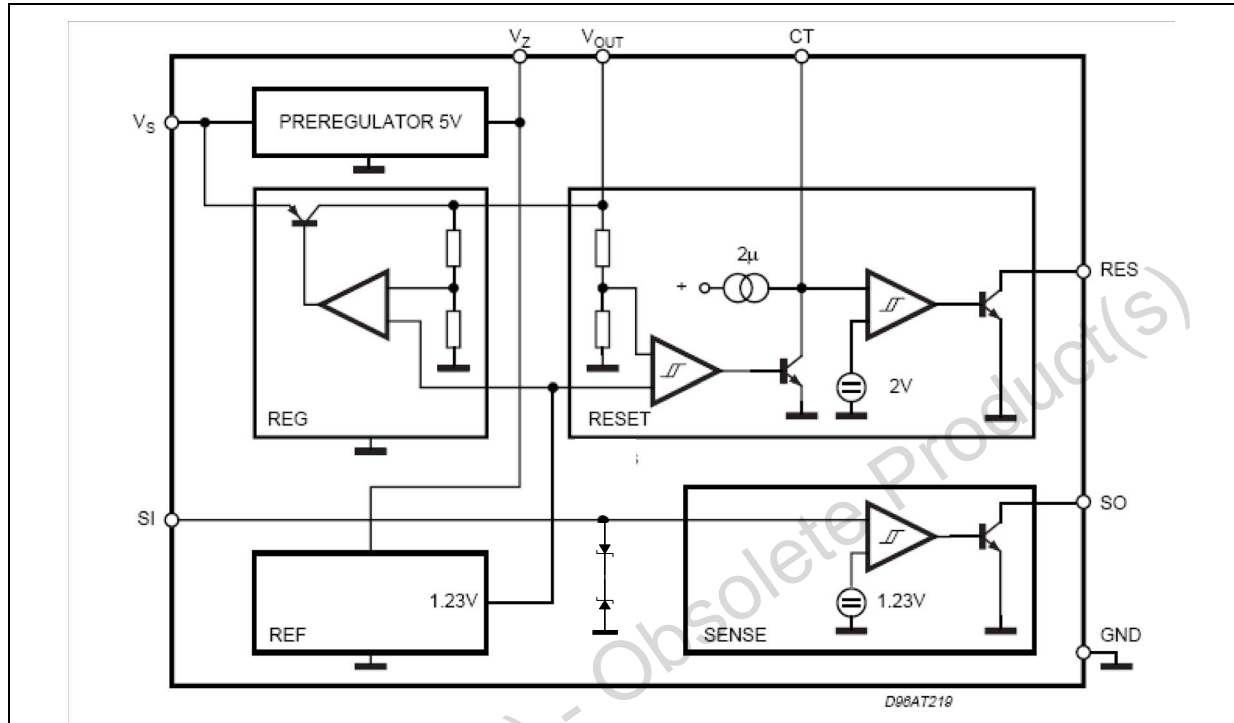
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Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram and pin description

Figure 1. Block diagram



Note: The block diagram illustrates only a major internal device functionality and it is not intended to mimic any details of hardware design

Figure 2. Configuration diagram (top view)

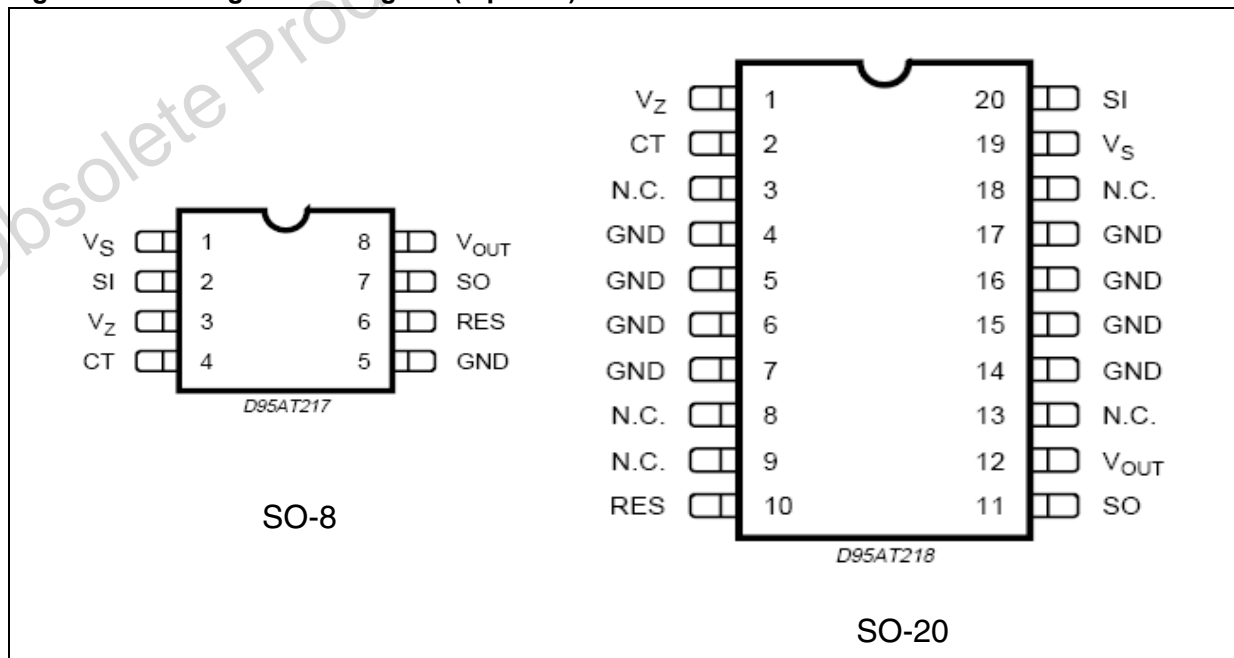


Table 2. Pin definitions and functions

Pin N°		Symbol	Function
SO-8	SO-20		
1	19	$V_S$	Input supply voltage. Block to GND via an external capacitor (see <a href="#">Figure 3</a> ).
2	20	$S_I$	Sense input pin to supervise input voltage. Connect via an external voltage divider connected to $V_S$ and to GND.
3	1	$V_Z$	Preregulator output voltage. For details, see <a href="#">Section 3.4: Preregulator</a> .
4	2	$C_T$	Reset pulse delay adjustment. Connecting this pin via a capacitor to GND
5	4, 5, 6, 7, 14, 15, 16, 17	GND	Ground reference
6	10	RES	Reset output. It is pulled down when the output voltage goes below $V_{RT}$ .
7	11	$S_O$	Sense output. This open collector pin must be connected to $V_{OUT}$ via an external resistor. It is pulled down whenever the $S_I$ voltage becomes lower than an internal voltage.
8	12	$V_{OUT}$	Output voltage. Block to GND via an external capacitor (see <a href="#">Figure 3</a> )
-	3, 8, 9, 13, 18	NC	Not connected pins

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>SDC</sub>	DC operating supply voltage	28	V
V <sub>STR</sub>	Transient supply voltage (T < 1s)	40	V
I <sub>O</sub>	Output current	Internally limited	
V <sub>O</sub>	Output voltage	20	V
V <sub>RES</sub> , V <sub>SO</sub>	Output voltage	20	V
I <sub>RES</sub> , I <sub>SO</sub>	Output current	5	mA
V <sub>CT</sub>	Reset delay voltage	7	V
V <sub>SIDC</sub>	Sense input voltage	28	V
V <sub>Z</sub>	Preregulator output voltage	7	V
I <sub>Z</sub>	Preregulator output current	5	mA
T <sub>J</sub>	Junction temperature	-40 to +150	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

1. The circuit is ESD protected according to MIL-STD-883C.

### 2.2 Thermal data

Table 4. Thermal data

Symbol	Description	SO-8	SO20L	Unit
R <sub>th j-amb</sub>	Thermal Resistance Junction-ambient (max)	200	50	°C/W
R <sub>th j-pins</sub>	Thermal Resistance Junction-pins (max)		15	°C/W
T <sub>JSD</sub>	Thermal Shutdown Junction temperature	165		°C

## 2.3 Electrical characteristics

$V_S = 14\text{ V}$ ;  $-40\text{ °C} < T_J < 125\text{ °C}$  unless otherwise specified

**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_O$	Output voltage	$T_J = 25\text{ °C}$ ; $I_O = 1\text{ mA}$	4.95	5	5.05	V
$V_O$	Output voltage	$6\text{ V} < V_{IN} < 28\text{ V}$ , $1\text{ mA} < I_O < 50\text{ mA}$	4.90	5	5.10	V
$V_O$	Output voltage	$V_{IN} = 40\text{ V}$ ; $T < 1\text{ s}$ ; $5\text{ mA} < I_O < 100\text{ mA}$	4.75		5.25	V
$V_{DP}$	Dropout voltage	$I_O = 10\text{ mA}$		0.1	0.25	V
		$I_O = 50\text{ mA}$		0.2	0.4	V
		$I_O = 100\text{ mA}$		0.3	0.5	V
$V_{IO}$	Input to output voltage difference in undervoltage condition	$V_{IN} = 4\text{ V}$ , $I_O = 35\text{ mA}$			0.4	V
$I_{\text{outh}}^{(1)}$	Max output leakage	$V_{IN} = 25\text{ V}$ , $V_O = 5.5\text{ V}$	20	50	80	$\mu\text{A}$
$V_{OL}$	Line regulation	$6\text{ V} < V_{IN} < 28\text{ V}$ ; $I_O = 1\text{ mA}$			20	mV
$V_{OLO}$	Load regulation	$1\text{ mA} < I_O < 100\text{ mA}$			30	mV
$I_{LIM}$	Current limit	$V_O = 4.5\text{ V}$	105	200	400	mA
		$V_O = 4.5\text{ V}$ ; $T_J = 25\text{ °C}$	120		400	mA
		$V_O = 0\text{ V}^{(2)}$		100		mA
$I_{QSE}$	Quiescent current	$I_O = 0.3\text{ mA}$ ; $T_J < 100\text{ °C}$		200	300	$\mu\text{A}$
$I_Q$	Quiescent current	$I_O = 100\text{ mA}$			5	mA

1. With this test we guarantee that with no output current the output voltage will not exceed 5.5V

2. Foldback characteristic

**Table 6. Reset**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{RT}$	Reset threshold voltage			$V_O - 0.5\text{ V}$		V
$V_{RTH}$	Reset threshold hysteresis		50	100	200	mV
$t_{RD}$	Reset pulse delay	$C_T = 100\text{ nF}$ ; $T_R \geq 100\text{ }\mu\text{s}$	55	100	180	ms
$V_{RL}$	Reset output low voltage	$R_{RES} = 10\text{ K}\Omega$ to $V_O$ $V_S \geq 1.5\text{ V}$			0.4	V
$I_{RH}$	Reset output high leakage current	$V_{RES} = 5\text{ V}$			1	$\mu\text{A}$
$V_{CTth}$	Delay comparator threshold			2		V
$V_{CTth, hy}$	Delay comparator threshold hysteresis			100		mV



Table 7. Sense

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{st}$	Sense low threshold		1.16	1.23	1.35	V
$V_{sth}$	Sense threshold hysteresis		20	100	200	mV
$V_{SL}$	Sense output low voltage	$V_{SI} \leq 1.16 \text{ V}; V_S \geq 3 \text{ V}$ $R_{SO} = 10 \text{ K}\Omega \text{ to } V_O$			0.4	V
$I_{SH}$	Sense output leakage	$V_{SO} = 5 \text{ V}; V_{SI} \geq 1.5 \text{ V}$			1	$\mu\text{A}$
$I_{SI}$	Sense input current	$V_{SI} = 0$	-20	-8	-3	$\mu\text{A}$

Table 8. Preregulator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_Z$	Preregulator output voltage	$I_Z = 10 \mu\text{A}$	4.5	5	6	V
$I_Z$	Preregulator output current				10	$\mu\text{A}$

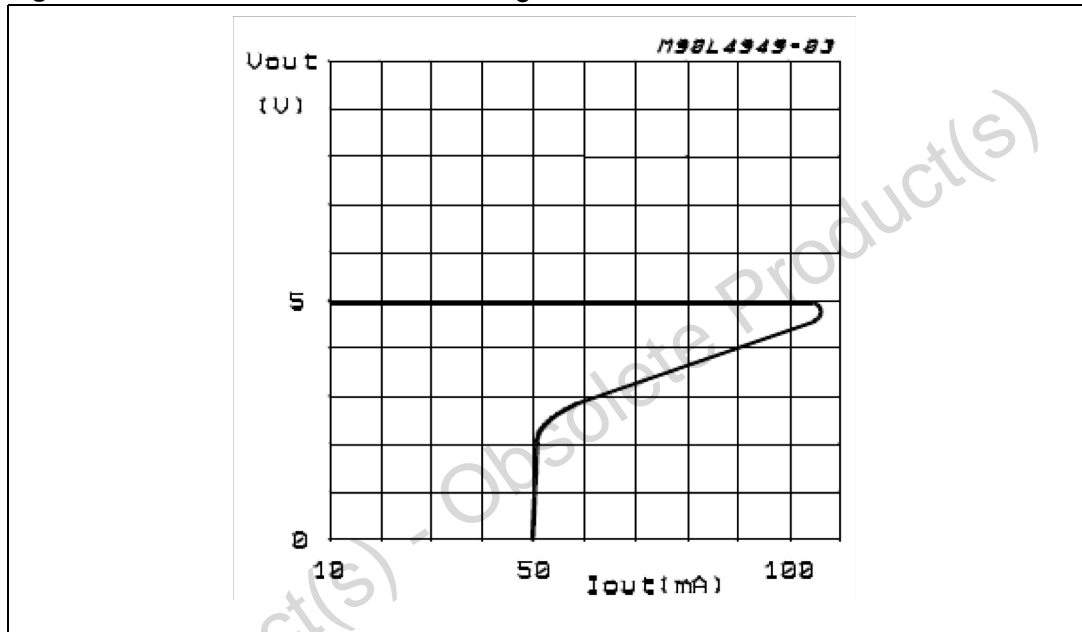


required. The modular approach of this device allows to get easily also other features and functions when required.

### 3.3 Voltage regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element.

**Figure 4. Foldback characteristic of  $V_O$**



With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. With this feature no functional interruption due to overvoltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage is shown in [Figure 5](#). The current consumption of the device (quiescent current) is less than 300  $\mu A$ .

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in [Figure 6](#).

Figure 5. Output voltage vs input voltage

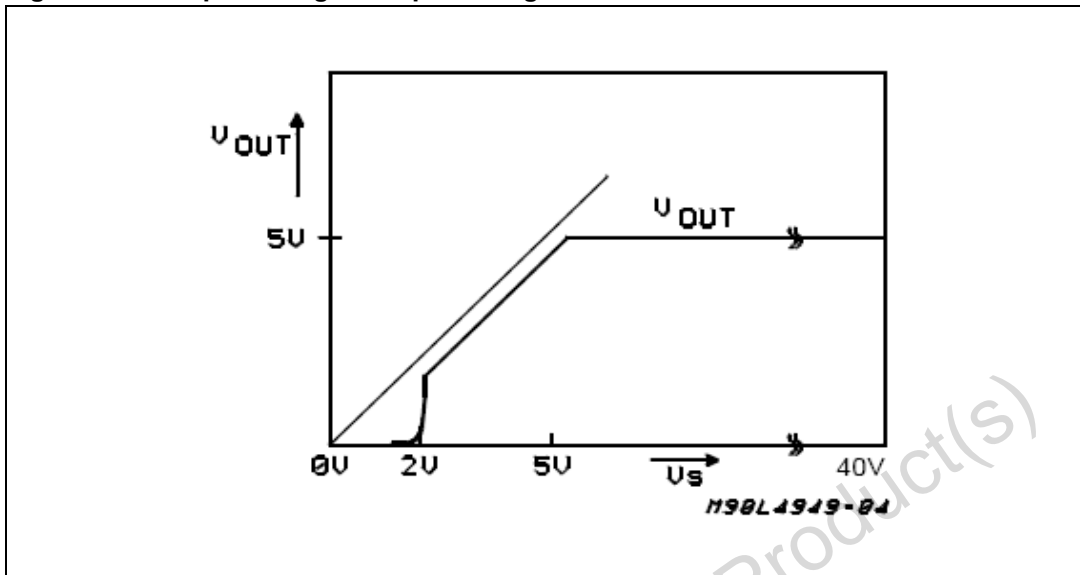
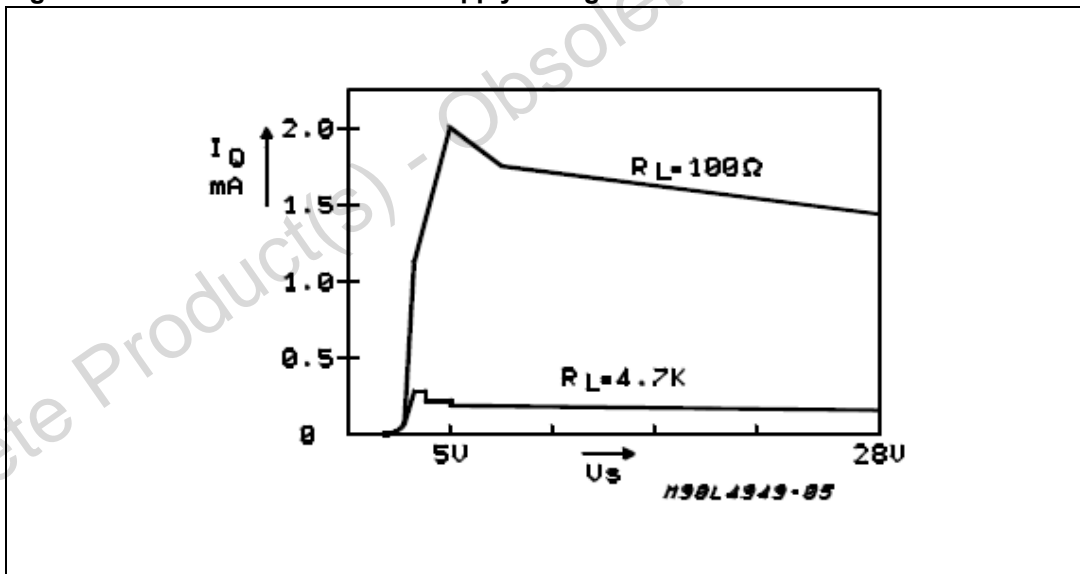


Figure 6. Quiescent current vs supply voltage



### 3.4 Preregulator

To improve the transient immunity a preregulator stabilizes the internal supply voltage to 5 V. This internal voltage is present at Pin 3 ( $V_Z$ ). This voltage should not be used as an output because the output capability is very small ( $\leq 10 \mu A$ ).

This output may be used as an option when a better transient behaviour for supply voltages less than 8 V is required (see also application note).

In this case a capacitor (100 nF - 1  $\mu F$ ) must be connected between pin  $V_Z$  and GND. If this feature is not used pin  $V_Z$  must be left open.

### 3.5 Reset circuit

The block circuit diagram of the reset circuit is shown in [Figure 7](#). The reset circuit supervises the output voltage.

The reset threshold of 4.5 V is defined with the internal reference voltage and standby output driver.

The reset pulse delay time  $t_{RD}$ , is defined with the charge time of an external capacitor  $C_T$ :

$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor  $C_T$  and is proportional to the value of  $C_T$ .

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time is generated for standby output voltage drops longer than approximately 50ms.

The typical reset output waveforms are shown in [Figure 8](#).

### 3.6 Sense comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

**Figure 7. Block circuit of reset circuit**

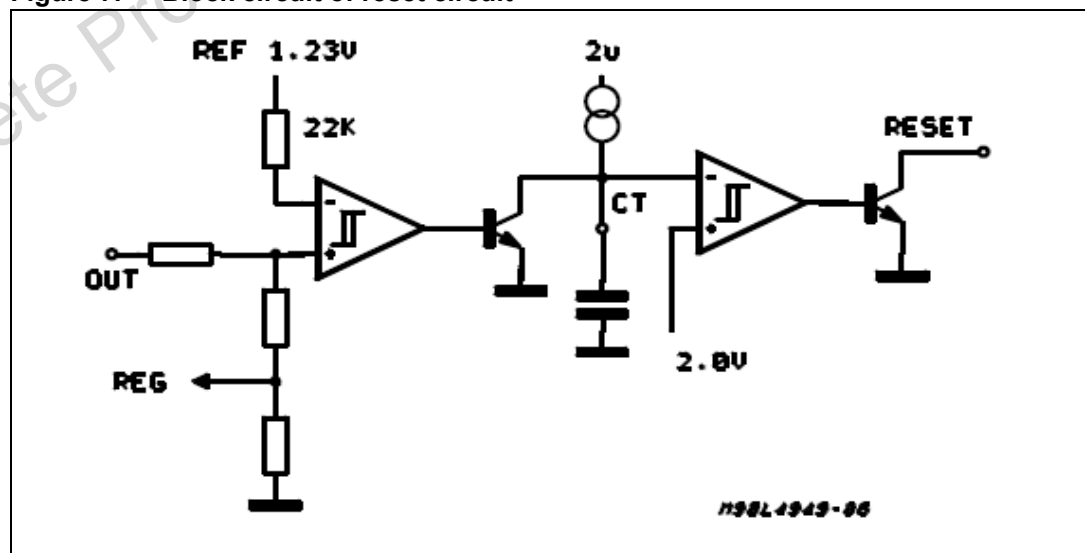
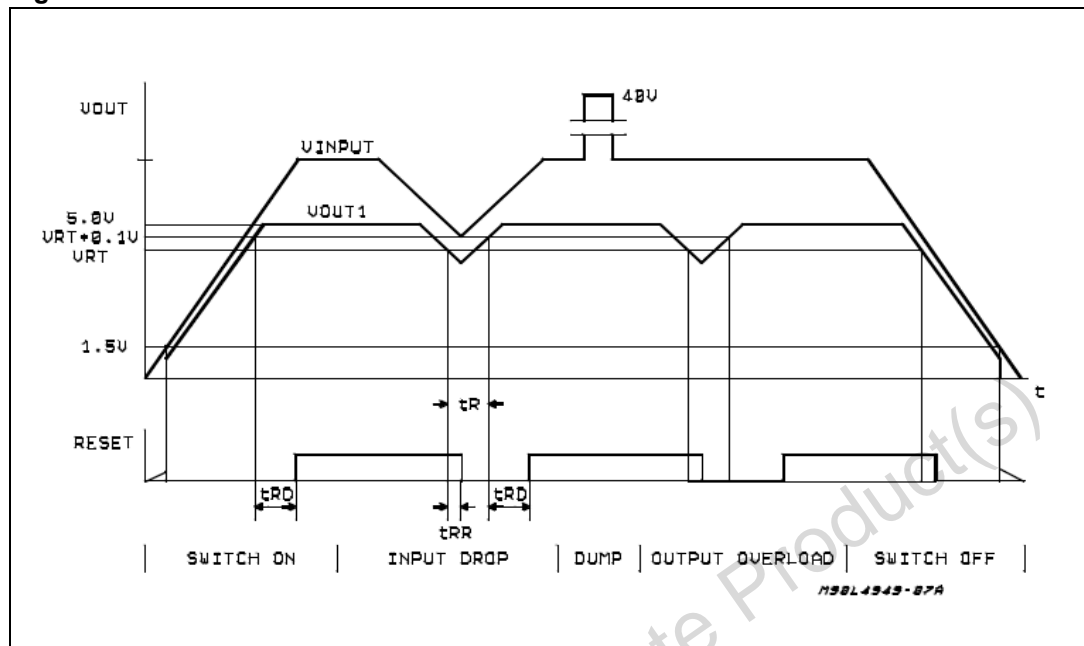


Figure 8. Waveforms



## 4 Package and packing information

### 4.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

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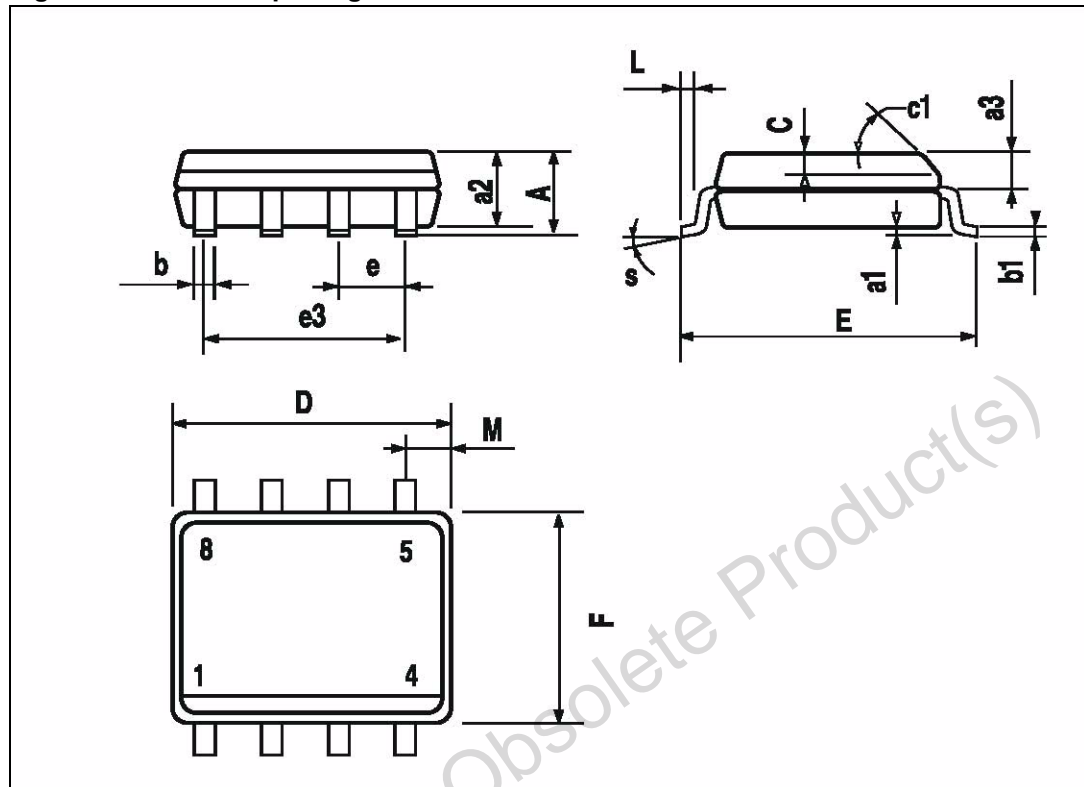
### 4.2 SO-8 TP package information

Table 9. SO-8 TP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45° (typ.)		
D <sup>(1)</sup>	4.8		5.0
E	5.8		6.2
e		1.27	
e3		3.81	
F <sup>(1)</sup>	3.8		4.0
L	0.4		1.27
M			0.6
S	8° (max.)		

1. D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).

Figure 9. SO-8 TP package dimensions



### 4.3 SO-20 TP package information

Table 10. SO-20 TP mechanical data

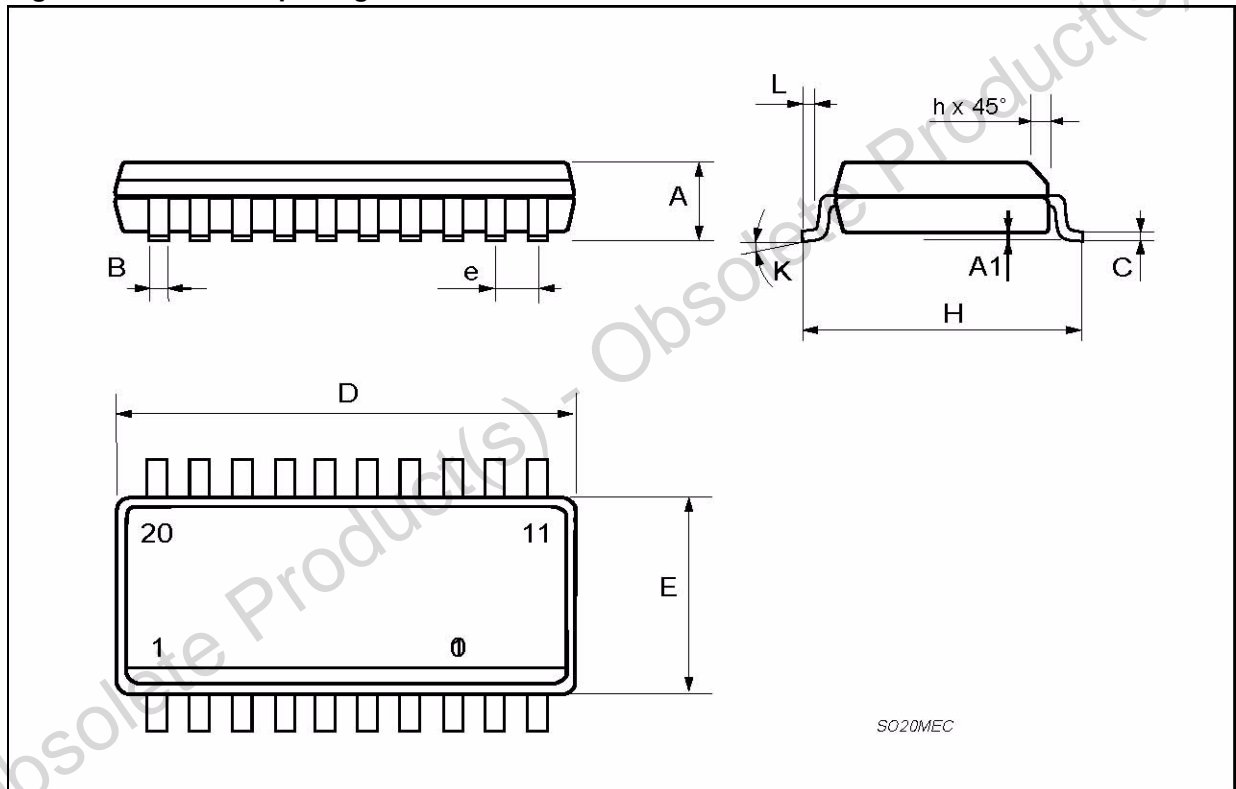
Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.1		0.3
B	0.33		0.51
C	0.23		0.32
D	12.6		13
E	7.4		7.6
e		1.27	
H	10		10.65



Table 10. SO-20 TP mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
h	0.25		0.75
L	0.4		1.27
K	0 (min.)8 (max.)		

Figure 10. SO20 TP package dimensions



## 5 Revision history

Table 11. Document revision history

Date	Revision	Description of changes
01-Jun-2000	1	Initial release.
25-Nov-2009	6	Reformatted entire document. Removed Minidip package. Added <a href="#">Table 2: Pin definitions and functions</a> . Updated <a href="#">Table 3: Absolute maximum ratings</a> Updated <a href="#">Figure 1: Block diagram</a> and <a href="#">Figure 3: Application circuit<sup>(1)</sup></a>

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