PAL22V10 Family, AmPAL22V10/A

24-Pin TTL Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 7.5-ns propagation delay and 91 MHz f_{MAX} (external)**
- **10 Macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-Pin SKINNYDIP, 24-pin Flatpack and 28-pin PLCC and LCC packages save space**

GENERAL DESCRIPTION

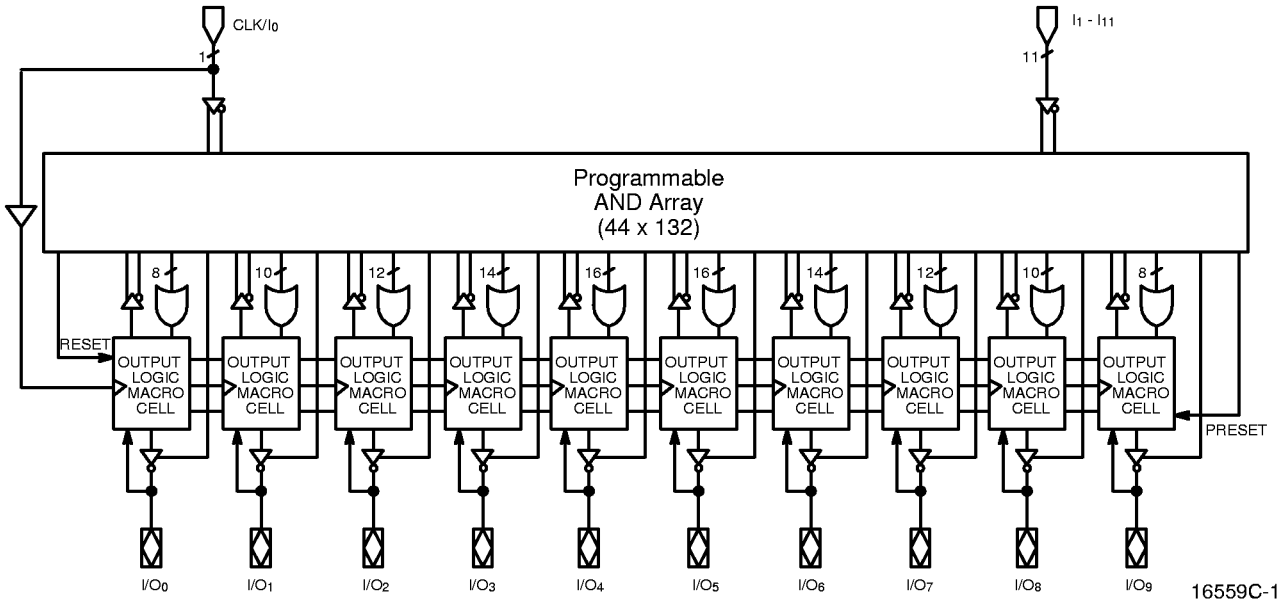
The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PAL22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.

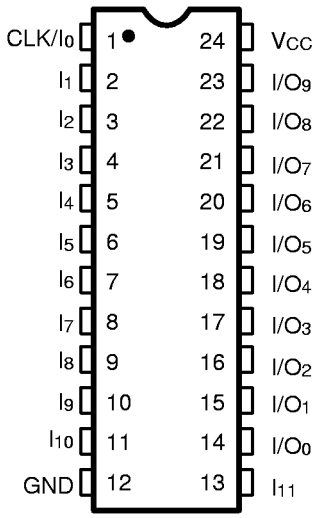
BLOCK DIAGRAM



CONNECTION DIAGRAMS

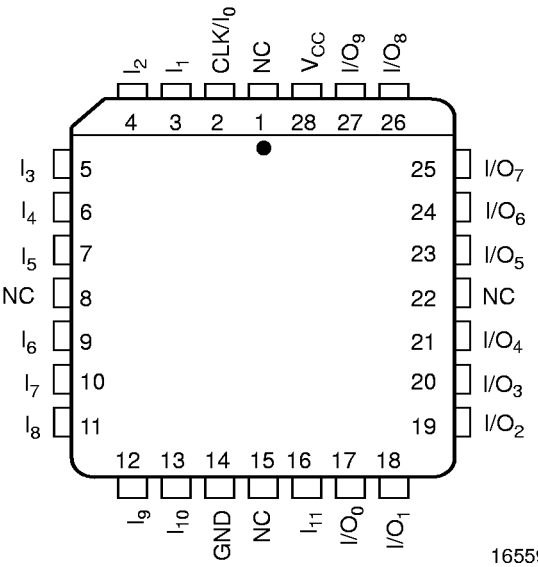
Top View

SKINNYDIP/FLATPACK



16559C-2

PLCC/LCC



16559C-3

Note:

Pin 1 is marked for orientation.

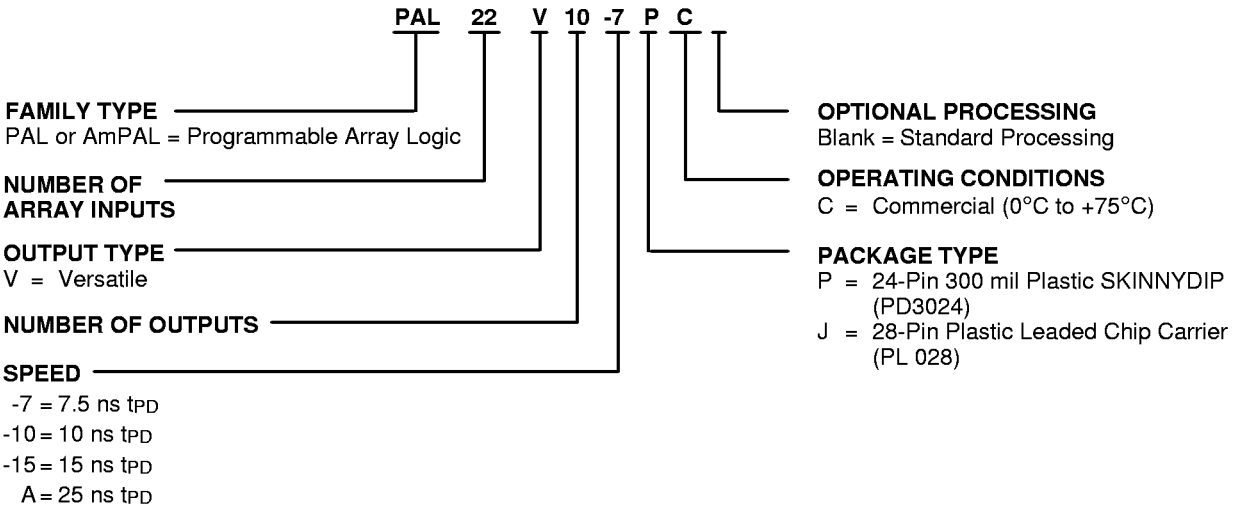
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-7	PC, JC
PAL22V10-10	
PAL22V10-15	
AmPAL22V10A	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PAL22V10 allows the systems engineer to implement a design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

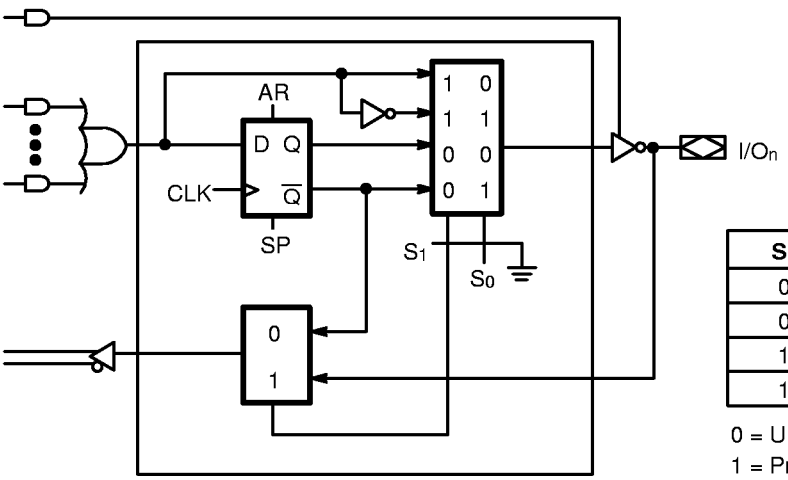
Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 – S_1. Multiplexer controls initially are connected to ground (0) through a programmable fuse, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse
1 = Programmed fuse

16559C-4

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

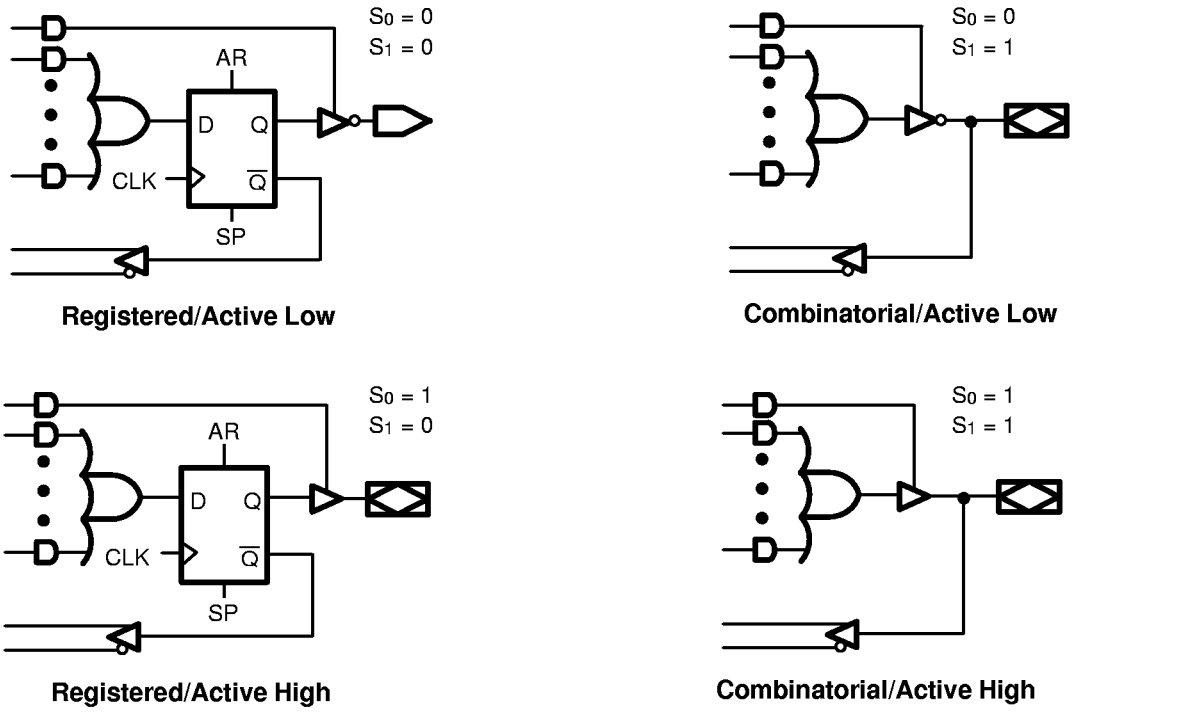


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions.

Preset/Reset

For initialization, the PAL22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

Programming

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed at the end of this data book.

Quality and Testability

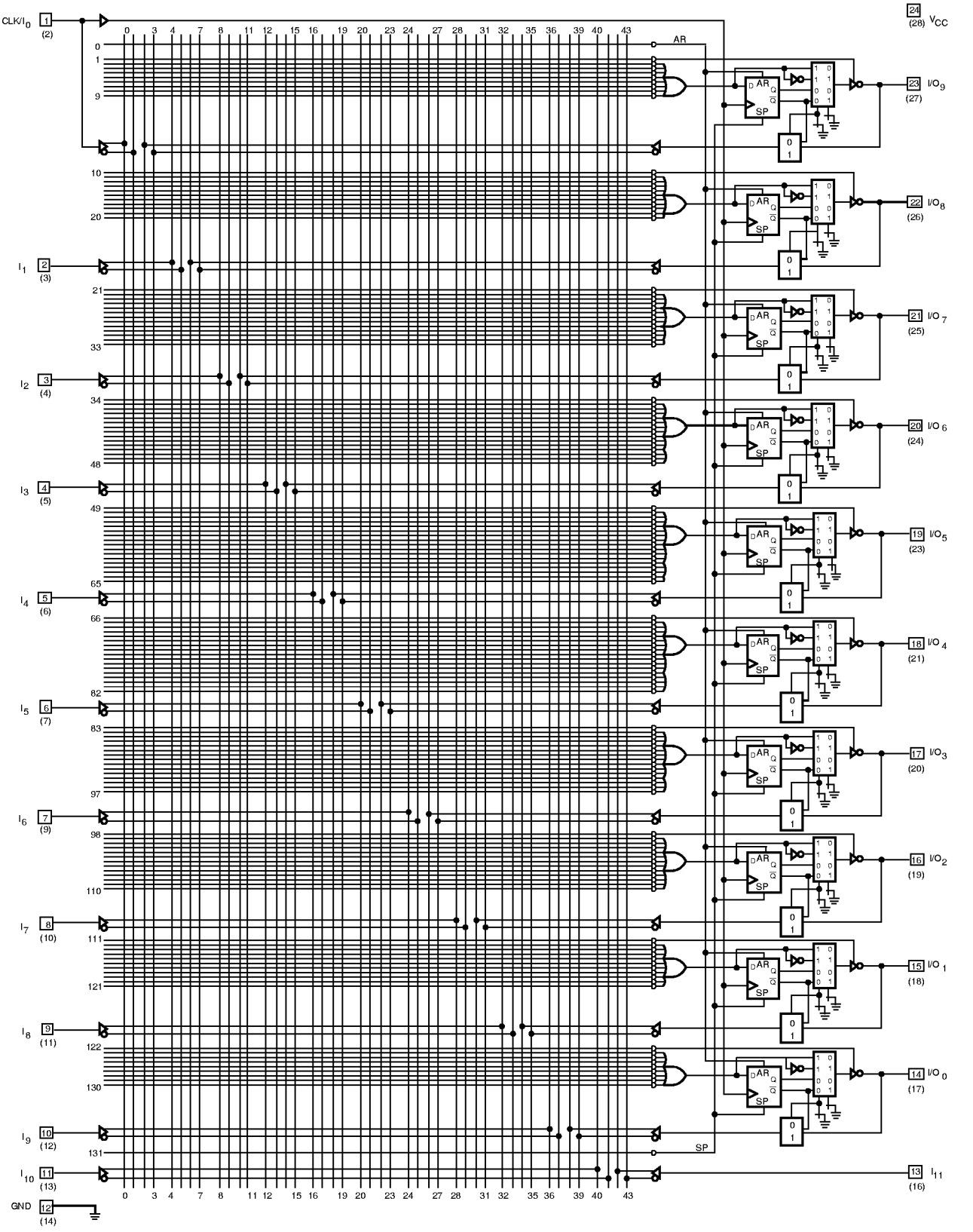
The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses, test words and test columns provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL22V10A is fabricated with AMD's diffusion-isolated bipolar process. The array connections are formed with highly reliable PtSi fuse.

The PAL22V10-15, -10 and -7 are fabricated with AMD's diffusion-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with PtSi fuses on the -15, and TiW fuses on the -7 and -10 for reliable operation.

LOGIC DIAGRAM
SKINNYDIP (PLCC/LCC) Pinouts



16559C-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with
Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.2 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)	Input		–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max			220	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	ns
t_S	Setup Time from Input, Feedback or SP to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	6	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 5)				1	ns
t_{AR}	Asynchronous Reset to Registered Output				12	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			5		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	91		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 6)	100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				8	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *Skew is measured with all outputs switching in the same direction.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with
Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.2 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)	Input		–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max			180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	7	ns
t_{AR}	Asynchronous Reset to Registered Output				15	ns
t_{ARW}	Asynchronous Reset Width			10		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	71		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		MHz
t_{EA}	Input to Output Enable Using Product Term Control				11	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Input Current . . . . . –30 mA to +5 mA

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		6	
				5	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to +5.5 V

DC Input Current . . . . . –30 mA to +5 mA

DC Output or I/O Pin Voltage . . . –0.5 V to V_{CC} Max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	11	pF
				6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

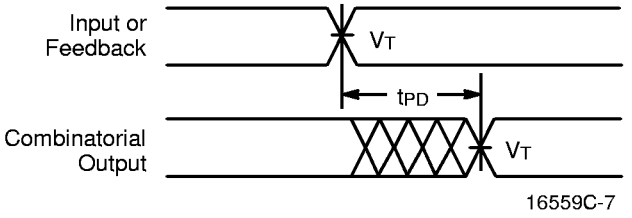
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				30	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			35		ns
t_{SPR}	Synchronous Preset Recovery Time			20		ns
t_{WL}	Clock Width	LOW		15		ns
t_{WH}		HIGH		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	28.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

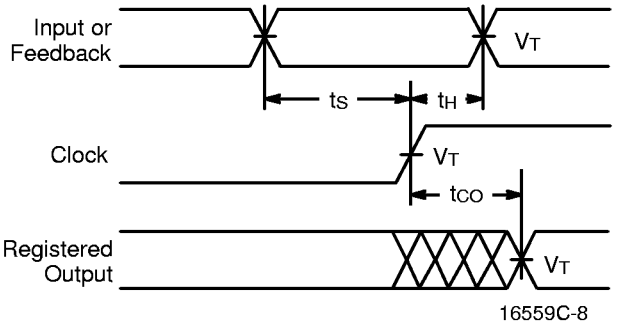
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

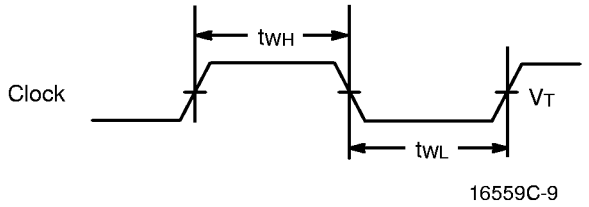
SWITCHING WAVEFORMS



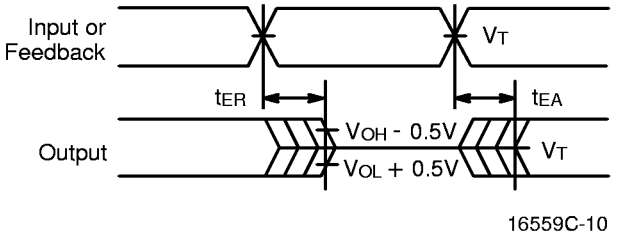
Combinatorial Output



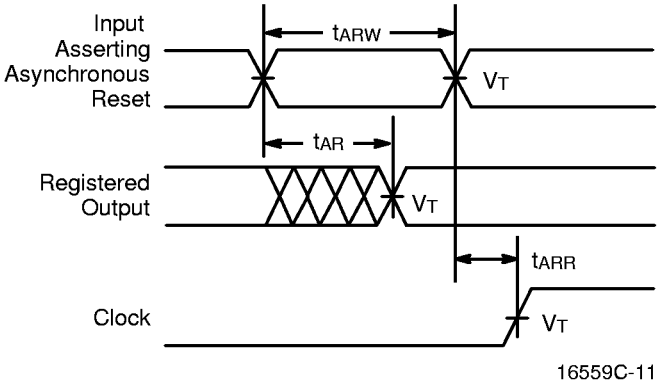
Registered Output



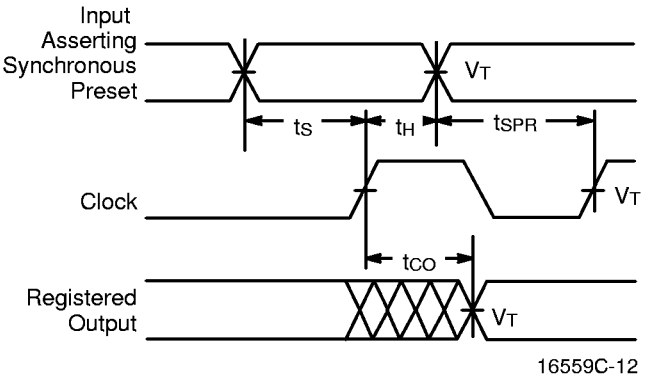
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

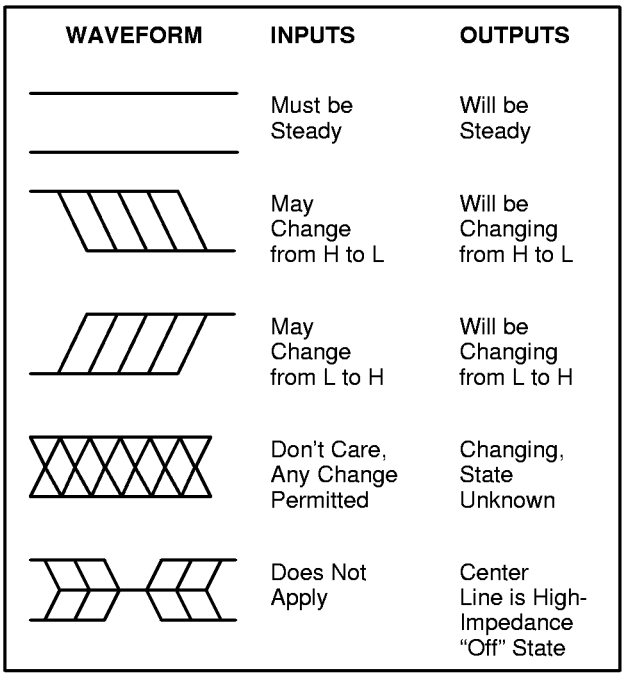


Synchronous Preset

Notes:

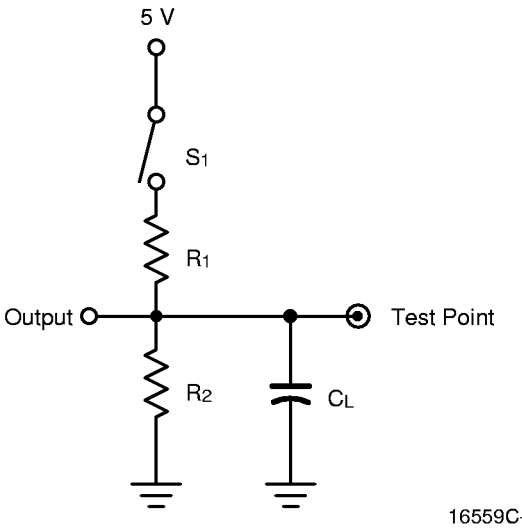
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 4 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT

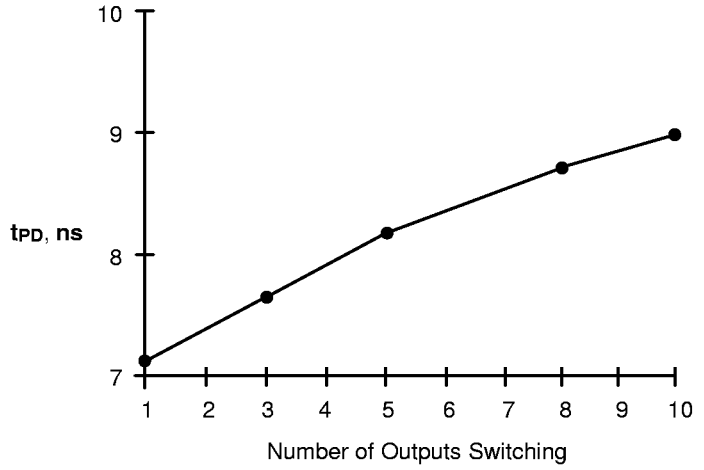


16559C-13

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	All except -7: 390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		-7: 300 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

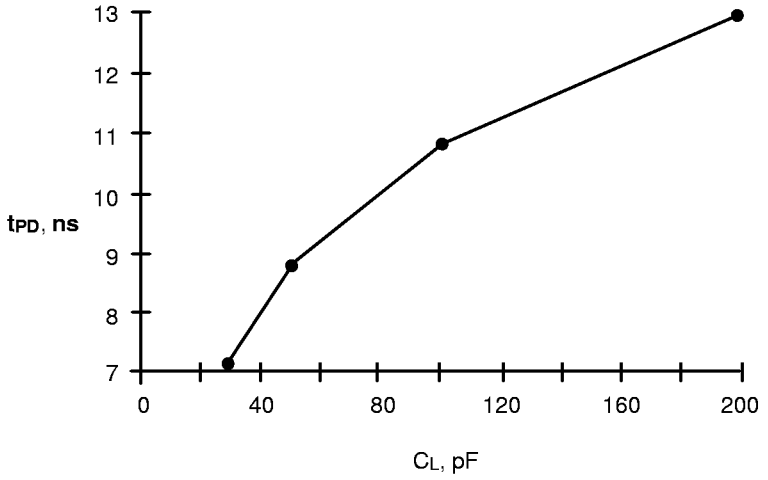
MEASURED SWITCHING CHARACTERISTICS for the PAL22V10-10

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

16559C-14



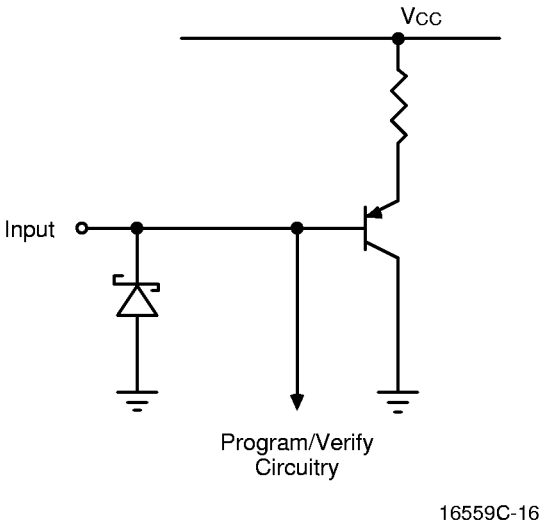
t_{PD} vs. Load Capacitance

16559C-15

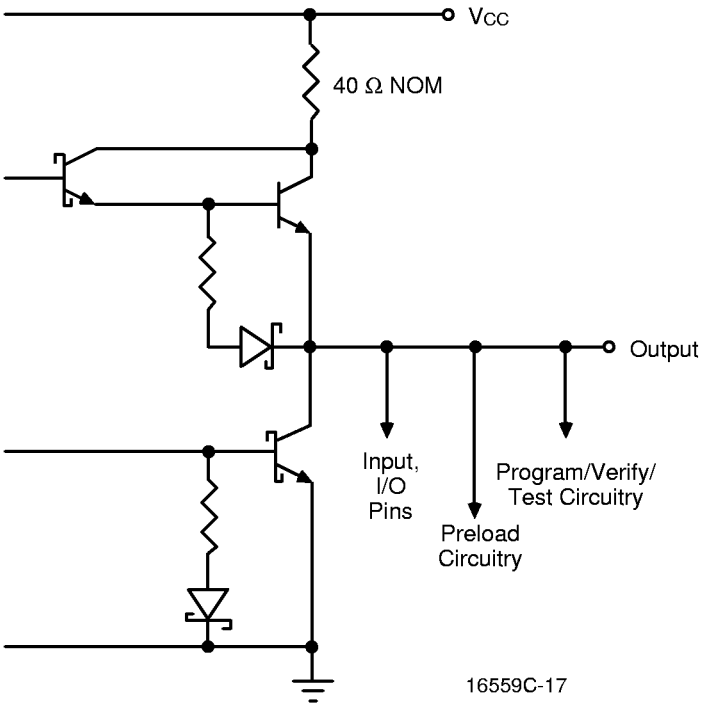
Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



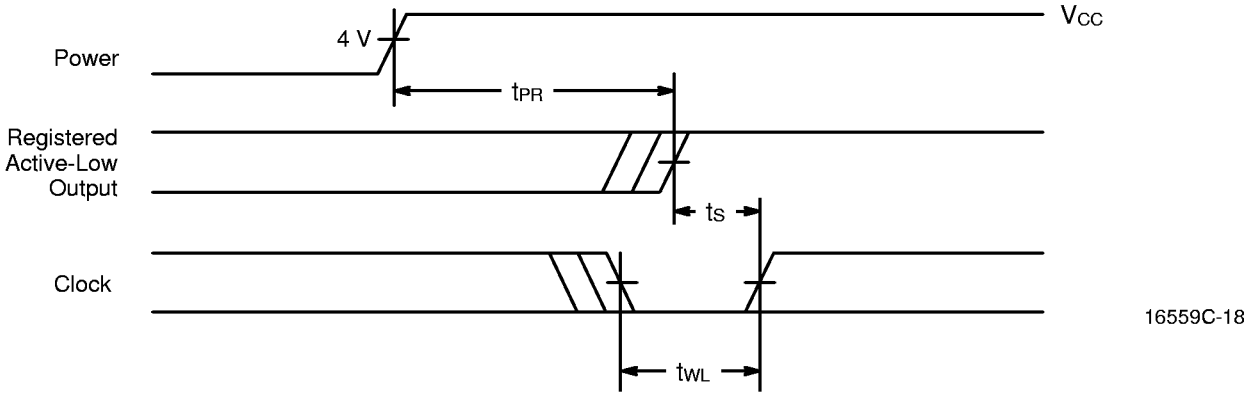
Typical Output

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

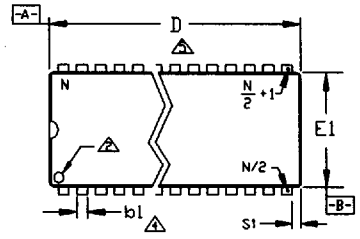
- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		

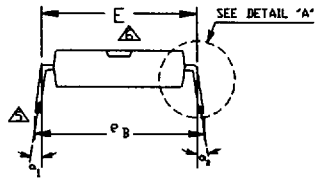


Power-Up Reset Waveform

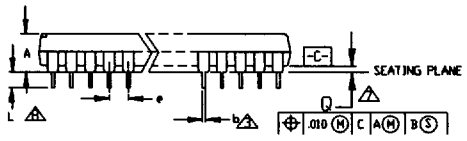
▶ Plastic Dual In Line (PDIP) Packages



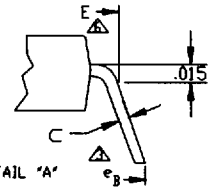
TOP VIEW



END VIEW



SIDE VIEW



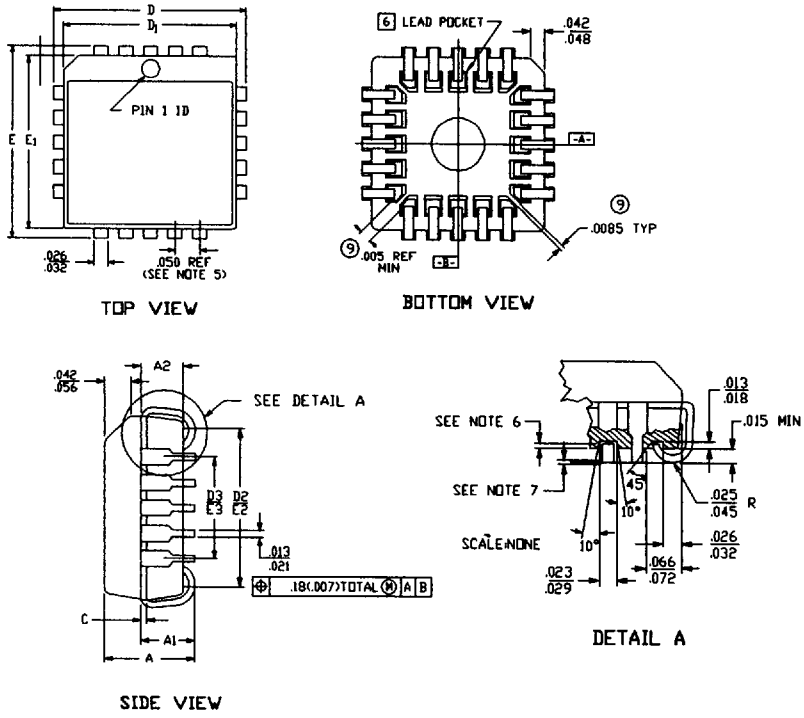
DIMENSION CODES	AMD PACKAGE TYPE & LEADCOUNT (JEDEC DRAWING NUMBER)							
	PD 022		PD 024		PD3024		PDW024	
	(MS-010(C)AA)		(MS-011(B)AA)		(MS-011(B)AA)		(MO-095(A)AG)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.140	0.200	0.140	0.225	0.140	0.200	0.140	0.200
b	0.014	0.022	0.014	0.022	0.014	0.022	0.014	0.022
b1	0.045	0.065	0.045	0.065	0.045	0.065	0.045	0.065
C	0.008	0.015	0.008	0.015	0.008	0.015	0.008	0.015
D	1.090	1.120	1.240	1.280	1.150	1.270	1.175	1.220
E1	0.340	0.380	0.520	0.580	0.240	0.280	0.240	0.290
E	0.390	0.430	0.600	0.625	0.300	0.325	0.300	0.330
L	0.120	0.160	0.120	0.160	0.120	0.160	0.120	0.160
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
Q	0.015	0.060	0.015	0.060	0.015	0.060	0.015	0.060
S1	0.005	—	0.005	—	0.005	—	0.005	—
e_b	0.430	0.500	0.630	0.700	0.330	0.430	0.330	0.430
$(\alpha_1 - \alpha_2)$	0°	10°	0°	10°	0°	10°	0°	10°
(α_1, α_2)	0°	15°	0°	15°	0°	15°	0°	15°
N	22		24		24		24	

Notes:

1. All dimensions are in inches.
2. A notch, tab, or pin one identification mark shall be located adjacent to the device pin one.
3. Lead thickness increases by a maximum of 0.003 inch when a solder lead finish is applied.
4. The minimum limit for the "b1" dimension is 0.030 inch in four corner leads for the PD 016, PD3024, PDW024, PD3028, and PDW028 package versions.
5. Dimensions "D" and "E1" do not include mold flash or protrusion.
6. Dimension "E" is measured from the outside of the leads and 0.015 inch below the plane of the package exit, as defined by the top of the lead.
7. Dimension "Q" is measured from the seating plane to the base plane.
8. Dimension "L" is measured from the seating plane (or from the lowest point of the lead shoulder width that measures 0.040 inch) to the lead tip.
9. The difference between these two dimensions should not exceed seven degrees.
10. When standoff has radii, the seating plane location is defined where the lead width equals 0.040 inch.
11. PD is AMD's internal designator for a plastic dual-in-line package. PD3 and PDW designate PDIP packages with package widths that differ from the standard width for that pin-count size.

▶ Plastic Leaded Chip Carrier (PLCC) Packages

Square Packages



DIMENSION CODES	AMD PACKAGE TYPE & LEADCOUNT (JEDEC DRAWING NUMBER)											
	PL 020		PL 028, PLH028		PL 044		PL 052		PL 068, PLH068		PL 084, PLH084	
	(MS-018(A)AA)		(MS-018(A)AB)		(MS-018(A)AC)		(MO-047(A)AD)		(MO-047(B)AE)		(MO-047(B)AF)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.180
A1	0.090	0.120	0.090	0.120	0.090	0.120	0.090	0.130	0.090	0.130	0.090	0.130
A2	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083	0.062	0.083
D, E	0.385	0.395	0.485	0.495	0.685	0.695	0.785	0.795	0.985	0.995	1.185	1.195
D1, E1	0.350	0.356	0.450	0.456	0.650	0.656	0.750	0.756	0.950	0.956	1.150	1.156
D2, E2	0.290	0.330	0.390	0.430	0.590	0.630	0.690	0.730	0.890	0.930	1.090	1.130
D3, E3	0.200 REF		0.300 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF	
C	0.009	0.015	0.009	0.015	0.009	0.015	0.009	0.015	0.007	0.013	0.007	0.013

Notes:

1. All dimensions are in inches.
2. Dimensions "D" and "E" are measured from the outermost point.
3. Dimensions "D1" and "E1" do not include corner mold flash. Allowable corner mold flash is 0.010 inch.
4. Dimensions "A, A1, D2, and E2" are measured from the points of contact to the base plane.
5. Lead spacing as measured from the center-line to the center-line shall be within ±0.005 inch.
6. J-bend lead tips should be located inside the "pockets."
7. Lead coplanarity shall be within 0.004 inch as measured from the seating plane.
8. Lead tweeze shall be within 0.0045 inch on each side as measured from a vertical flat plane.
9. The lead pocket may be rectangular (as shown) or oval. If the corner lead pockets are connected, then 0.005-inch minimum lead spacing is required.
10. PL is AMD's internal abbreviation for a PLCC. PLH refers to one that has been thermally enhanced with an embedded heat spreader.