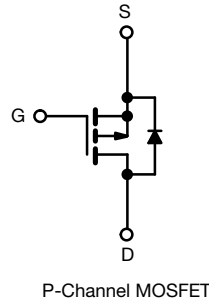


Power MOSFET



P-Channel MOSFET

FEATURES

- Dynamic dv/dt rating
- Repetitive avalanche rated
- For automatic Insertion
- End stackable
- P-channel
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY

V_{DS} (V)	-100	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.60
Q_g max. (nC)	18	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	9.0	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD9120PbF

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	-100	V	
Gate-source voltage	V_{GS}	± 20		
Continuous drain current	V_{GS} at -10 V	$T_A = 25$ °C	-1.0	A
		$T_A = 100$ °C	-0.70	
Pulsed drain current ^a	I_{DM}	-8.0		
Linear derating factor		0.0083	W/°C	
Single pulse avalanche energy ^b	E_{AS}	140	mJ	
Repetitive avalanche current ^a	I_{AR}	-1.0	A	
Repetitive avalanche energy ^a	E_{AR}	0.13	mJ	
Maximum power dissipation	$T_A = 25$ °C	P_D	1.3	W
Peak diode recovery dv/dt ^c		dv/dt	-5.5	V/ns
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering rRecommendations (peak temperature) ^d	For 10 s		300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = -25$ V, starting $T_J = 25$ °C, $L = 52$ mH, $R_g = 25$ Ω , $I_{AS} = -2.0$ A (see fig. 12)
- $I_{SD} \leq -6.8$ A, $di/dt \leq 110$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C
- 1.6 mm from case



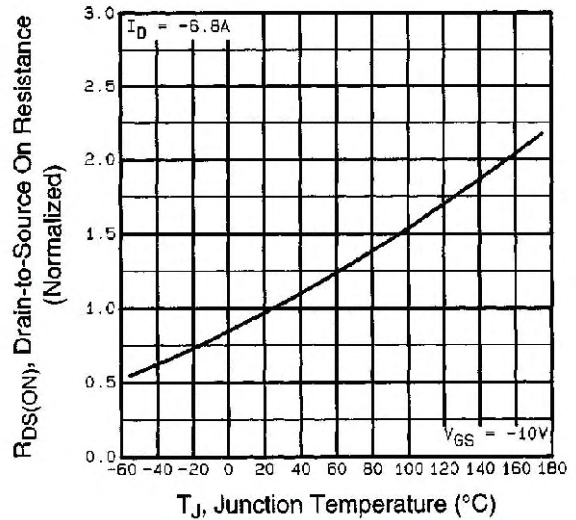
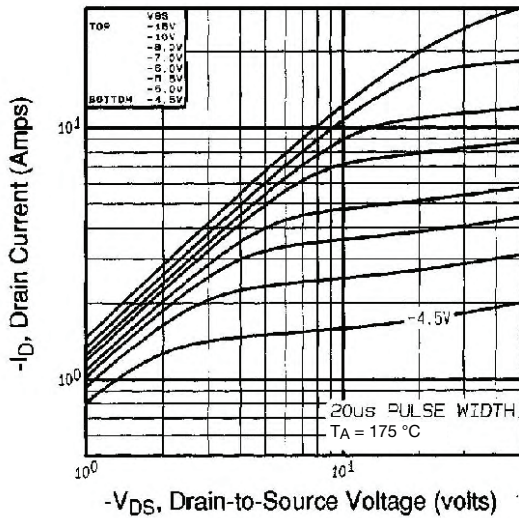
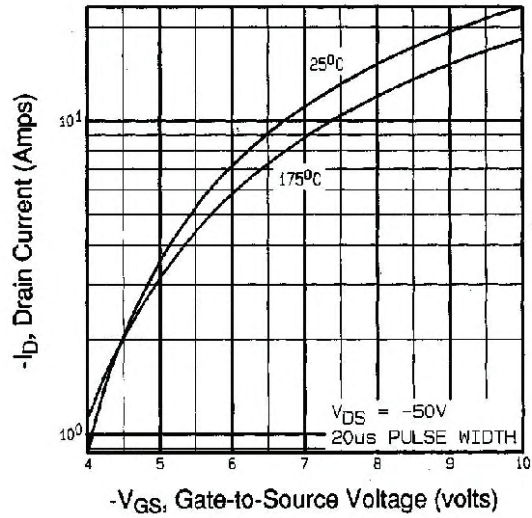
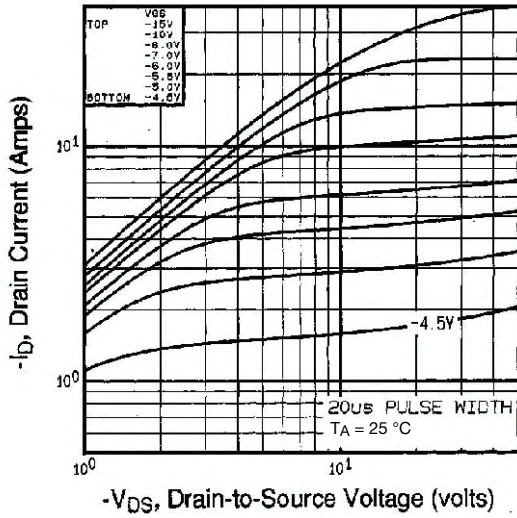
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	120	°C/W

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA		-100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.10	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	-500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -0.6 A ^b	-	-	0.60	Ω
Forward transconductance	g _{fs}	V _{DS} = -50 V, I _D = -0.60 A ^b		0.71	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = -25 V f = 1.0 MHz, see fig. 5		-	390	-	pF
Output capacitance	C _{oss}			-	170	-	
Reverse transfer capacitance	C _{rss}			-	45	-	
Total gate charge	Q _g	V _{GS} = -10 V	I _D = -6.8 A, V _{DS} = -80 V see fig. 6 and 13 ^b	-	-	18	nC
Gate-source charge	Q _{gs}			-	-	3.0	
Turn-on delay time	Q _{gd}			-	-	9.0	
Rise time	t _{d(on)}	V _{DD} = -50 V, I _D = -6.8 A R _g = 18 Ω, R _D = 7.1 Ω, see fig. 10 ^b		-	9.6	-	ns
Turn-off delay time	t _r			-	29	-	
Fall time	t _{d(off)}			-	21	-	
Turn-on delay time	t _f			-	25	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal source inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-1.0	A
Pulsed diode forward current ^a	I _{SM}			-	-	-8.0	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = -1.0 A, V _{GS} = 0 V ^b		-	-	-6.3	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = -6.8 A, di/dt = 100 A/μs ^b		-	98	200	ns
Body diode reverse recovery charge	Q _{rr}			-	0.33	0.66	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



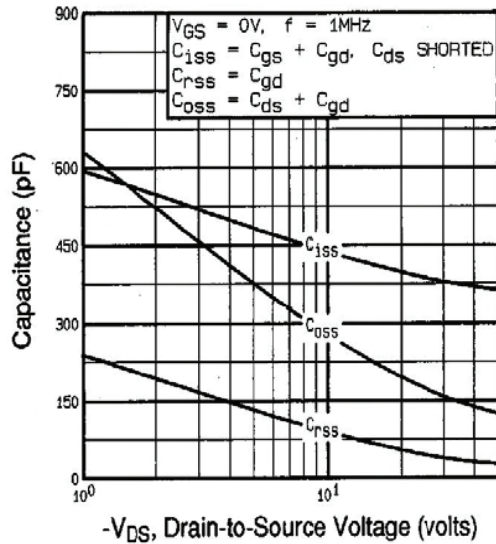


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

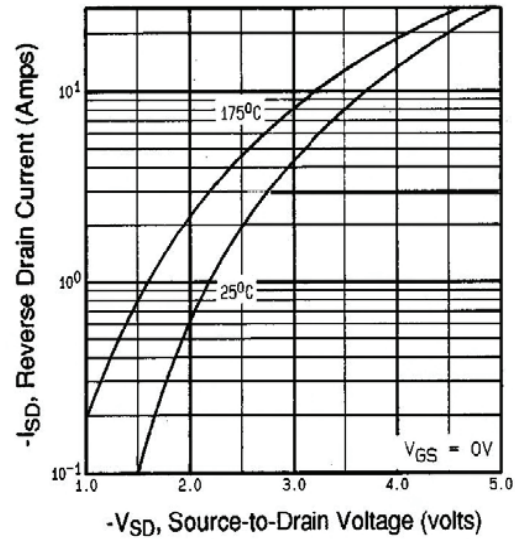


Fig. 7 - Typical Source-Drain Diode Forward Voltage

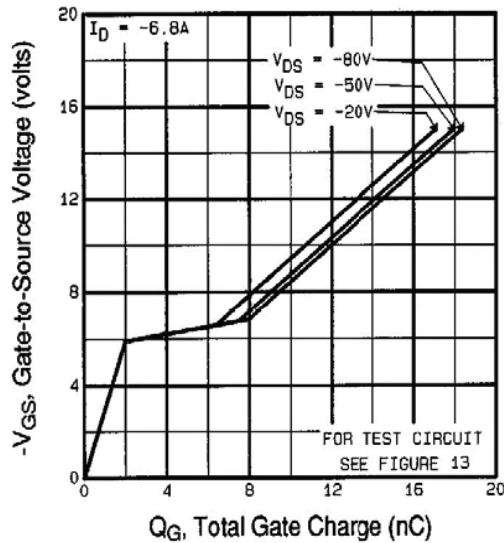


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

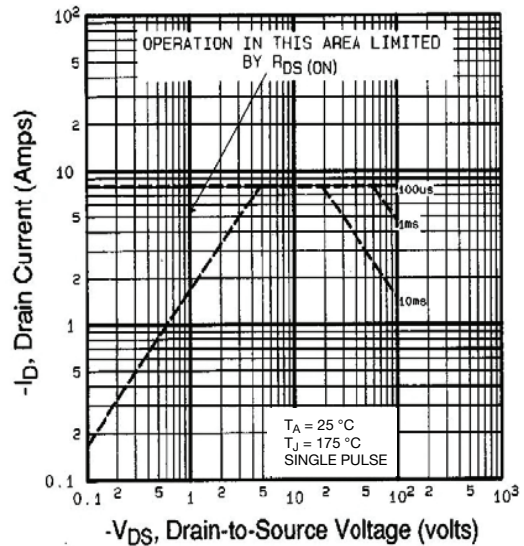


Fig. 8 - Maximum Safe Operating Area

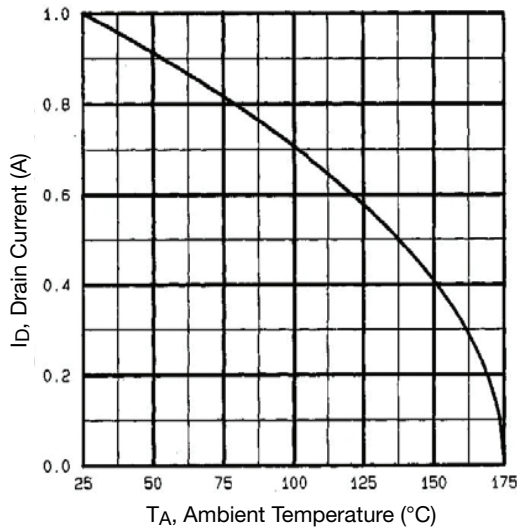


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

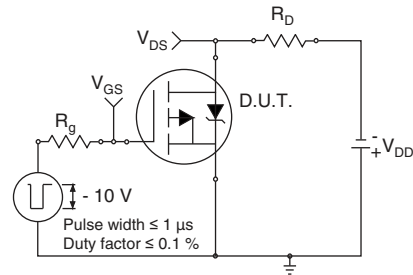


Fig. 10a - Switching Time Test Circuit

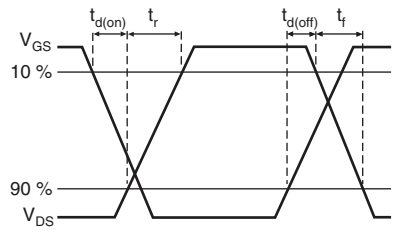


Fig. 10b - Switching Time Waveforms

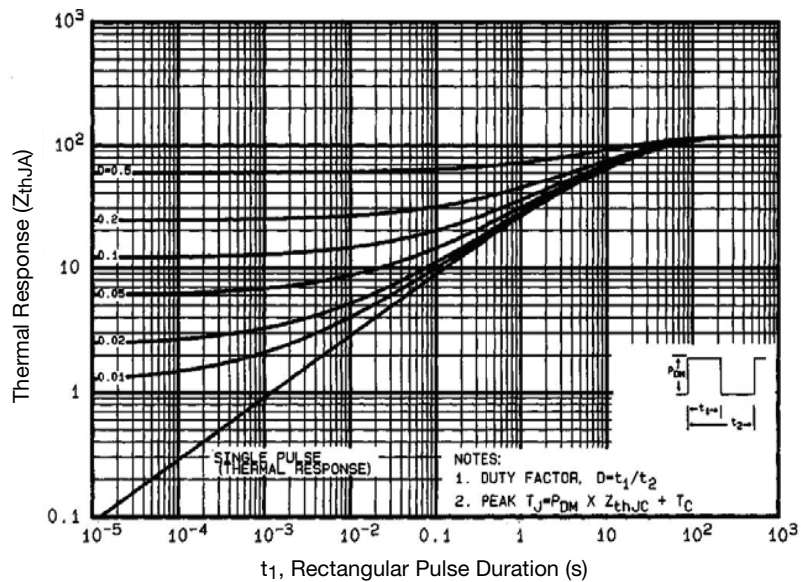


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

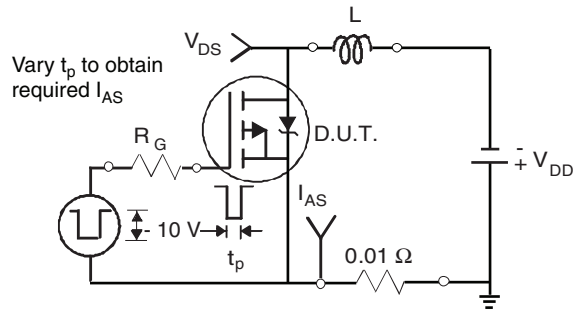


Fig. 12a - Unclamped Inductive Test Circuit

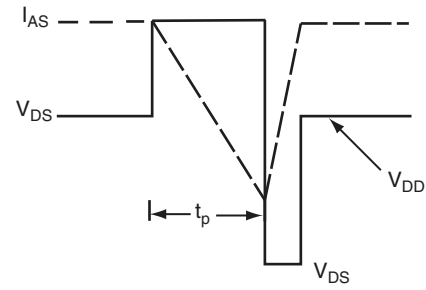


Fig. 12b - Unclamped Inductive Waveforms

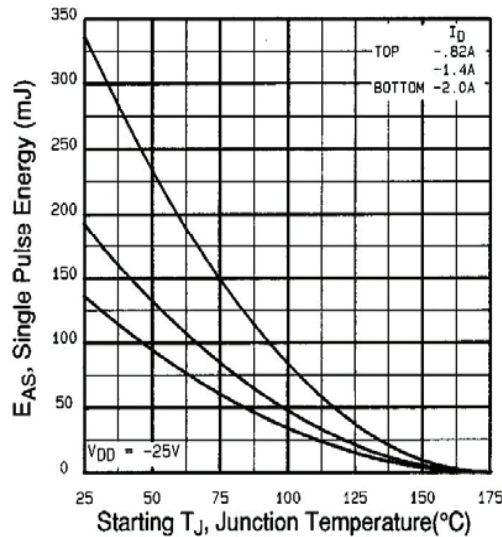


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

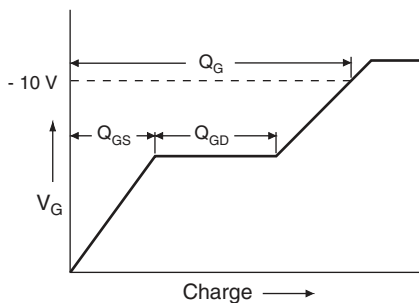


Fig. 13a - Basic Gate Charge Waveform

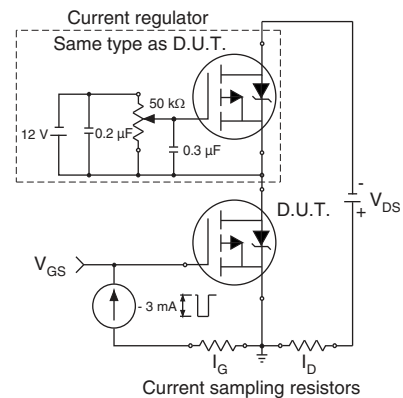
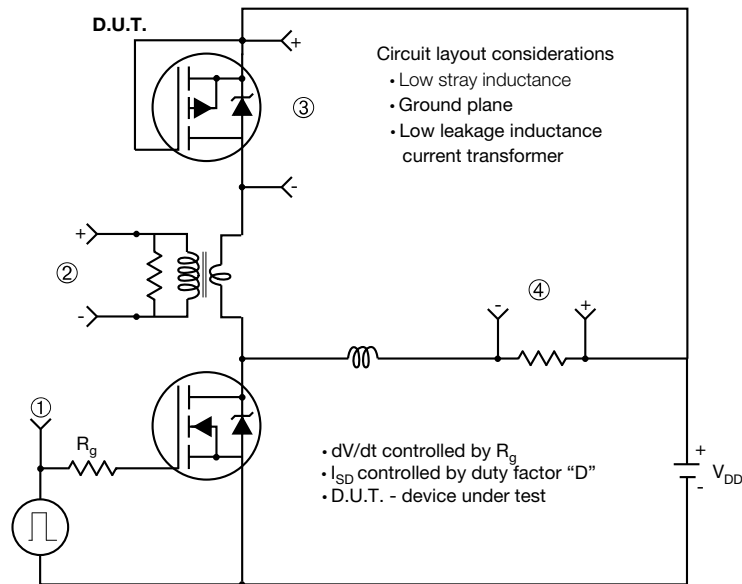
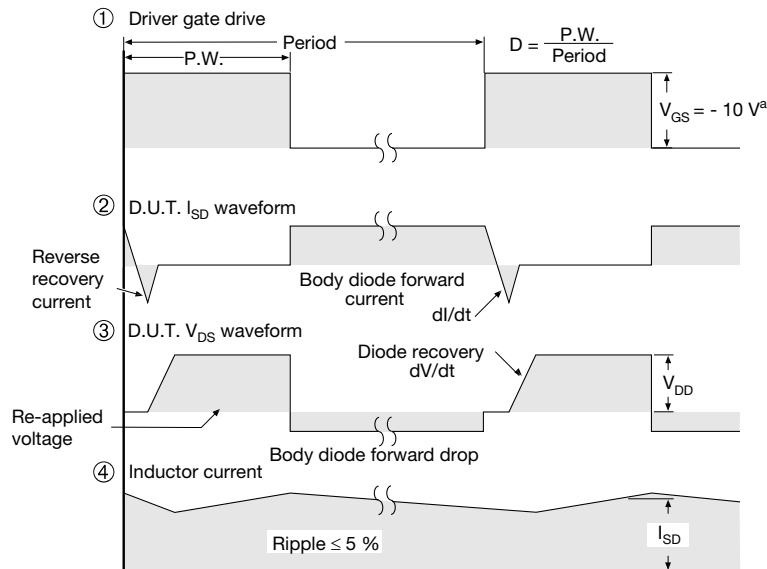


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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