Micro Power Inverting Charge Pump

- Low Power Voltage Conversion
- +2.4V to +5.5V Input Range
- 99% Voltage Conversion Efficiency
- Typical 60μA Supply Current
- Requires Only Three External Capacitors
- Includes Low Power Shutdown Option
- Ideal in Portable Applications Such As
  - Handheld Instruments
  - Cellular Phones
  - Personal Digital Assistants
  - Laptops and Notebooks
- Pin Compatible Upgrade to Microchip's TC682

APPLICATIONS

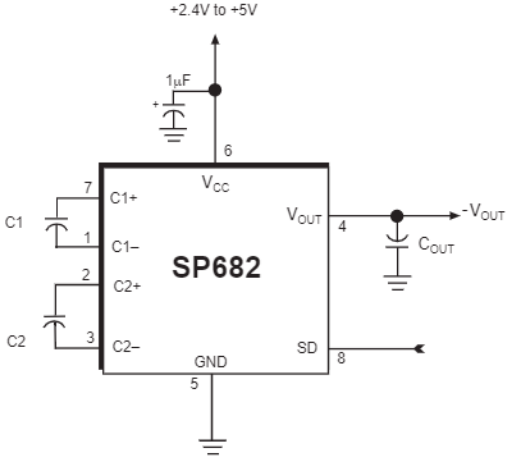
- LCD Display
- Negative bias supply for op amps
- Serial interface protocol circuits

DESCRIPTION

The **SP682** is a monolithic charge pump voltage converter that produces a doubled, negative voltage from a single positive supply. The **SP682** charge pump outputs a –10V voltage from a +5V input. Three external charge pump capacitors are required to support the voltage conversion and voltage doubling process. An internal oscillator generates a 12kHz clock which cycles the internal switching that charges the storage and transfer capacitors. The charge pump architecture is fabricated using a low power BiCMOS process technology.

The **SP682** charge pump is ideal for low power applications requiring a typical +3V battery source such as a lithium cell. Typical applications are handheld instruments, notebook and laptop computers, cellular phones, and data acquisition or GP systems. The **SP682** is packaged in either 8-pin NSOIC, 8-pin MSOP for surface mount applications, and 8 Pin PDIP.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +7V
V_{OUT} ..... –11V
Storage Temperature ..... -65°C to +150°C

Power Dissipation:
8-pin NSOIC 500mW
8-pin MSOP 320mW
8-pin PDIP 750mW
Package Derating:
8-pin NSOIC:
$ø_{JA}$ ..... 128 °C/W
8-pin MSOP:
$ø_{JA}$ ..... 216°C/W
8-pin PDIP:
$ø_{JA}$ ..... 97°C/W

ELECTRICAL CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX} and V_{CC} = +5V. Charge pump cap = 3.3µF, unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SUPPLY CURRENT					CHARGE PUMP CAPACITORS: 3.3µF
I_{CC}		60	120	µA	$R_L = \infty$, T_A = +25°C
			200	µA	$R_L = \infty$
in shutdown			1	µA	T_A = +25°C, SD = +5V
CHARGE PUMP OUTPUT					CHARGE PUMP CAPACITORS: 3.3µF
V_{OUT}	–9.9	–9.99		Volts	$R_L = \infty$
	–9.0	–9.5		Volts	R_L = 2kΩ
SOURCE RESISTANCE					
R_{OUT}		140	180	Ω	I_L = 10mA, T_A = +25°C
			230	Ω	I_L = 10mA
		380	450	Ω	I_L = 5mA, V_{CC} = +2.8V
OSCILLATOR FREQUENCY					
f_{OSC}		12	20	kHz	$f_{osc} = 2 X f_{C1+}$
CONVERSION EFFICIENCY					
$V_{OUT\ EFF}$	99	99.9		%	$R_L = \infty$
$V_{OUT\ EFF}$	90	95		%	R_L = 2kΩ
START-UP TIMING					
V_{OUT} Power On Delay		12		ms	R_L = 2kΩ
SHUTDOWN TIMING					
Shutdown to V_{OUT} Delay		5		ms	R_L = 2kΩ
SUPPLY VOLTAGE					
V_{CC}	+2.4		+5.5	Volts	
Operating Temperature Range					
- C	0		+70	°C	
- E	-40		+85	°C	

The **SP682**'s charge pump design is a simplified version of **Sipex**'s original patented charge pump design (5,306,954) except that it only generates a negative output. The charge pump utilizes external capacitors to store the charge. Figure 1 shows the waveform found on the negative side of capacitor C2. There is a free–running oscillator, running at 12kHz, that controls the two phases of the voltage shifting. A description of each phase follows.

Phase 1

V_{OUT} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

V_{OUT} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{OUT} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

The oscillator frequency or clock rate for the charge pump is designed for low power operation. The oscillator operates at a frequency of about 12kHz (20kHz maximum) which conserves power as opposed to higher frequency which operation typically draws more power from V_{CC}. The external charge pump capacitors specified are 3.3µF but the absolute minimum should be 1µF.

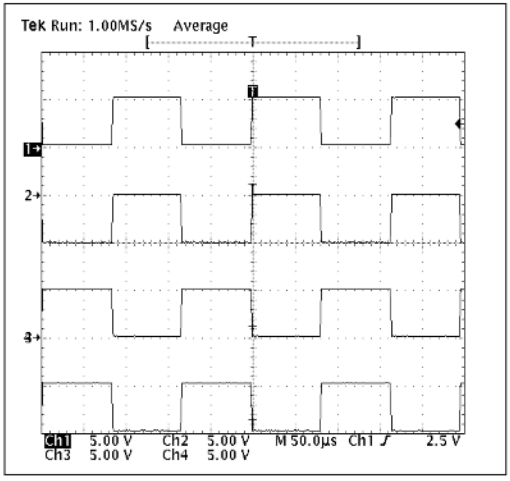


Figure 1. Charge Pump Waveform

EFFICIENCY INFORMATION

A charge pump theoretically produces a doubled voltage at 100% efficiency. However in the real world, there is a small voltage drop on the output which reduces the output efficiency. The **SP682** can usually run 99.9% efficient without driving a load. While driving a 1kΩ load, the **SP682** remains over 90% efficiency.

$$\text{Output Voltage Efficiency} = V_{OUT} / (-2 * V_{CC});$$

$$V_{OUT} = -2 * V_{CC} + V_{DROP}$$

$$V_{DROP} = (I_{OUT}) * (R_{OUT})$$

$$\text{Power Loss} = I_{OUT} * (V_{DROP})$$

The efficiency changes as the external charge pump capacitors are varied. Larger capacitor values will strengthen the output and reduce output ripple. Although smaller capacitors will cost less and save board space, lower values will reduce the output drive capability and also increase the output ripple.

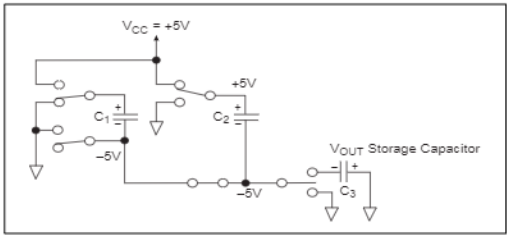


Figure 2. Charge Pump Phase 1

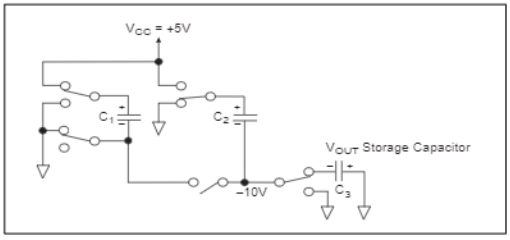


Figure 3. Charge Pump Phase 2

The ESR of the charge pump capacitors also determine the output resistance. Assuming that switch resistances are approximately equal, the output resistance can be derived as shown below:

$$R_{OUT} = 16*(R_{SW1-4}) + 4*(ESR_{C1} + ESR_{C2}) + ESR_{C3} + 1 / (f_{OSC} * C1) + 1 / (f_{OSC} * C2)$$

R_{OUT} is typically 140Ω at +25°C with VCC at +5V using 3.3μF capacitors. The total internal switch resistance ($16*R_{SW}$) is approximately 90Ω. The table below shows the comparison of R_{OUT} versus C1&C2.

C1, C2 (μF)	ROUT (Ω)
0.05	4085
0.10	2084
0.47	510
1.00	285
3.30	140
4.70	125
10.00	105
22.00	94

Table 1. R_{OUT} .vs. C1, C2

The output voltage ripple is also affected by the capacitors, specifically C_{OUT}. Larger values will reduce the output ripple for a given output current load of current. The formula representation is:

$$V_{RIPPLE} = \{1 / [2 * (f_{OSC} * C3)] + 2 * (ESR_{C3})\} * I_{OUT}$$

To minimize the output ripple, the C_{OUT} storage capacitor can be increased to over 10μF whereas the pump capacitors can range from 1μF to 5μF. *Table 2* shows the typical V_{RIPPLE} for given C_{OUT} values.

C_{OUT} (μF)	V_{RIPPLE} (mV)
0.50	1020
1.00	520
3.30	172
4.70	120
10.00	70
22.00	43

Table 2. C3 .vs. V_{RIPPLE}

SHUTDOWN FEATURE

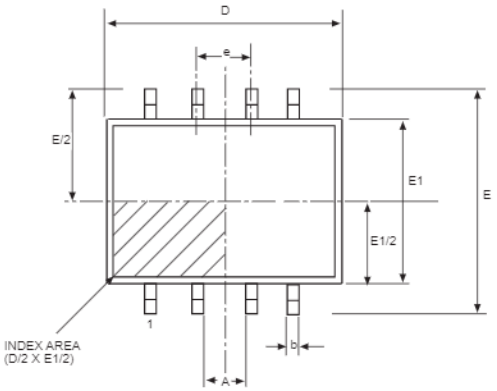
The **SP682** charge pump includes a shutdown feature (pin 8) which disables the charge pump when the V_{OUT} is not needed. A logic "1" will activate the shutdown mode. If shutdown is not needed, it can be left open where an internal pull-down resistor will always keep the charge pump active. Typical input current for the shutdown pin is 3μA. The shutdown feature is another option for conserving power in portable applications, reducing current to only 1μA.

PARALLEL DEVICES

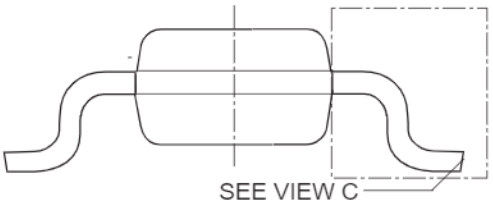
Multiple **SP682** charge pumps can be connected in parallel. However, the effective output resistance now is the output resistance of a single device divided by the number of devices. Connecting multiple pumps allows the user to save on the storage capacitor. The charge pump capacitors still must be separate for each device.

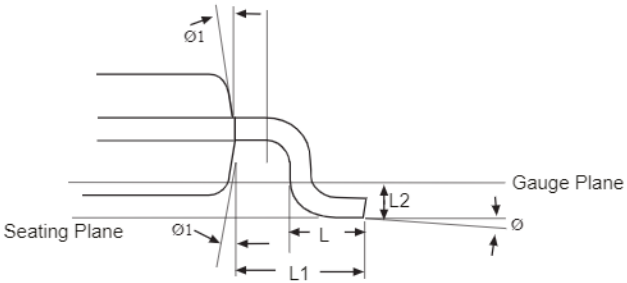
APPLICATIONS INFORMATION

The **SP682** charge pump produces a doubled, inverted voltage from the V_{CC} input. As such, it can serve in many applications where a negative –5V to –10V output is needed. Typical applications include powering analog switches, and biasing LCD displays and panels.

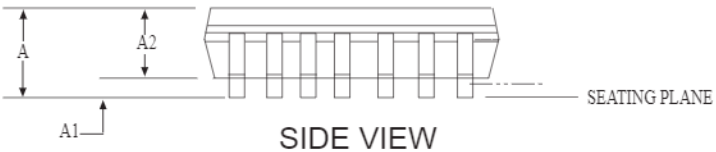


TOP VIEW



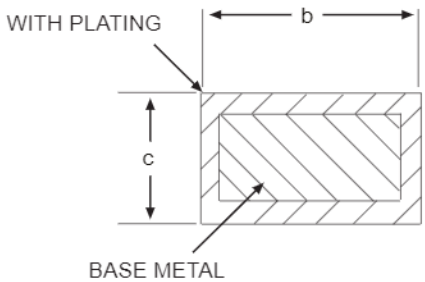


VIEW C



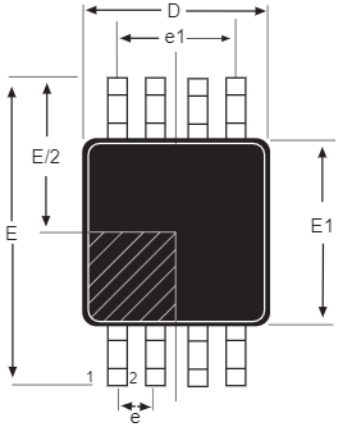
SIDE VIEW

DIMENSIONS Minimum/Maximum (mm)	8 Pin NSOIC (JEDEC MS-012, AA - VARIATION)		
COMMON HEIGHT DIMENSION			
SYMBOL	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
L2	0.25 BSC		
Ø	0º	-	8º
Ø1	5º	-	15º

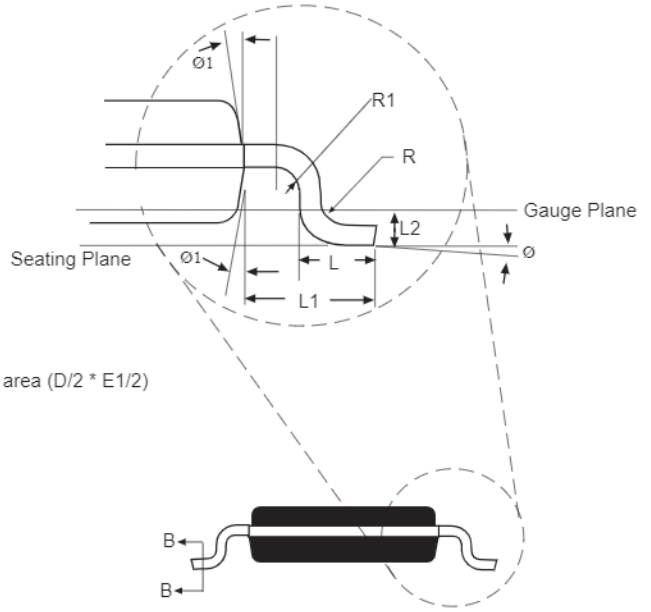


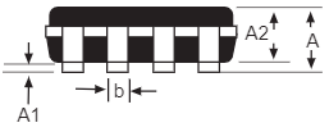
CONTACT AREA

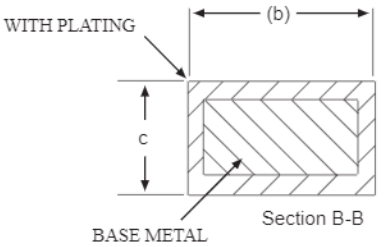
PACKAGE: 8 PIN NSOIC



Pin #1 indentifier must be indicated within this shaded area (D/2 * E1/2)

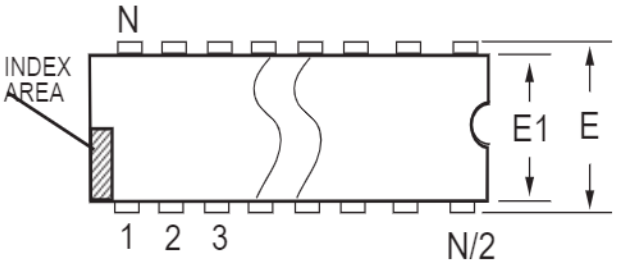


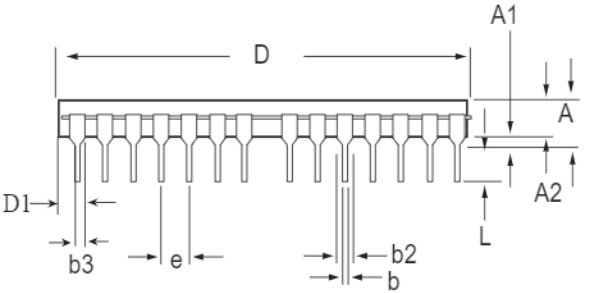


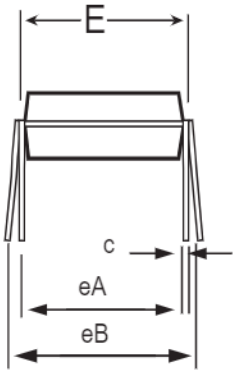


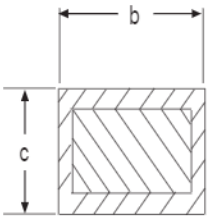
8-PIN MSOP JEDEC MO-187 (AA) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	1.10
A1	0	-	0.15
A2	0.75	0.85	0.95
b	0.22	-	0.38
c	0.08	-	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.65 BSC		
e1	1.95 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
N	-	8	-
R	0.07	-	-
R1	0.07	-	-
Ø	0°		8°
Ø1	0°	-	15°

8-PIN MSOP









8 PIN PDIP JEDEC MS-001 (BA) Variation	Dimensions in inches		
	MIN	NOM	MAX
A	-	-	.210
A1	.015	-	-
A2	.115	.130	.195
b	.014	.018	.022
b2	.045	.060	.070
b3	.030	.039	.045
c	.008	.010	.014
D	.355	.365	.400
D1	.005	-	-
E	.300	.310	.325
E1	.240	.250	.280
e	.100 BSC		
eA	.300 BSC		
eB	-	-	.430
L	.115	.130	.150

8 PIN PDIP

