AMD FT3 Based Gizmo 2 Development Board Schematic

NOTES:

1) This Mini-ITX form factor reference schematic is for AMD FT3 Processor based systems. It can be used as a starting point for any design that uses this processor.

2) Unless otherwise specified, resistors have 5% tolerance.

3) Unless otherwise specified, capacitors have 20% tolerance.

IMPORTANT NOTICE:

1) This document may not reflect the most recent changes in board development and debug. Any developer intending to use this documentation as a reference should contact Gizmosphere via www.gizmosphere.org for updates, design recommendations and PCB layout guidelines. Gizmosphere also recommends a design review before considering production.

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Cover Page

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REVISION HISTORY:

REV	DATE	NOTES
A	Mar 06, 2013	Initial Release
B	May 14, 2013	DVT Release
C	Aug 07, 2013	PVT Release
D	Nov 26, 2014	Page 8: Change APU_HSYNC to be pulled up to +3.3V. Page 9: a. Change R56 not to be populated. b. Change GBE_SMBALERT connected from GPIO68 to USB_OC2_L/TCK/GEVENT14_L for fixing two power domain of leakage problem. Page 17: Change R330 not to be populated for fixing two power domain of of leakage problem. Page 22: a. Change C352 not to be populated. b. Add R364, and change C318 to 4700pF. Page 23: a. Add an AND gate U133 with VDDIO_SUS_PWRGD and SLP_S3# inputs and the output to enable +5V, +3.3V, +1.8V and +0.95V. b. Remove R345, R335, R344 and R334. c. Add snubber circuit C353/R358 and C355/R363. d. Add 0 OHM resistor R359 and R362 to boot pin. Page 24: a. Add 33 OHM series resistors on APU_SVD, APU_SVC and APU_SVT. b. Change R278 connection from APU_VDDIO_SUS to +1.8V for fixing two power domain of leakage problem. Page 25: a. Remove R343 and R339. b. Add snubber circuit C354 and R361. d. Add 0 OHM resistor R360 to boot pin.

REFERENCE COLLATERAL:

The documents below were referenced in the creation of these schematics and were the published revisions at that time. They are listed here for reference only.

For the latest information, always visit www.gizmosphere.org.

PID	REV	TITLE
51492	0.90	AMD Electrical Data Sheet (EDS) for AMD Family 16h Models 00h-0Fh Processors (NDA)
51489	1.06	AMD FT3 Processor Functional Datasheet
51387	1.03	AMD FT3 Processor Motherboard Design Guide
51389	1.05	AMD FT3 Processor Motherboard Schematic Checklist
51388	1.02	AMD FT3 Processor Motherboard Layout Checklist
51814	1.01	AMD Thermal Design Guide for FT3 Processors
40821	1.62	AMD SB Temperature Sensor Interface (SB-TSI) Specification
48022	1.04	AMD Serial VID Interface 2.0 (SVI2) Specification
50818	1.00	AMD FT3 Infrastructure Roadmap

Revision History

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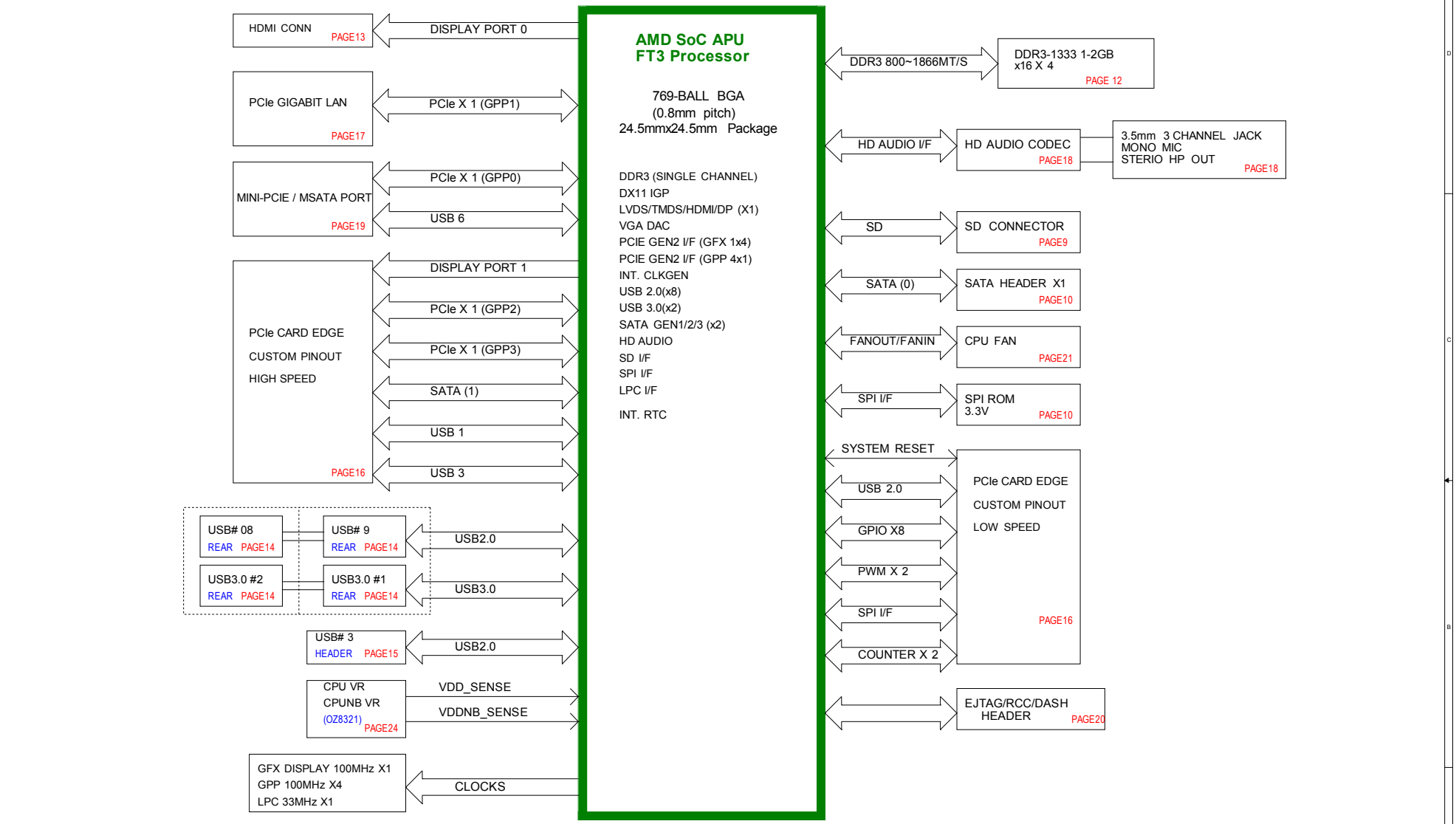

Block Diagram

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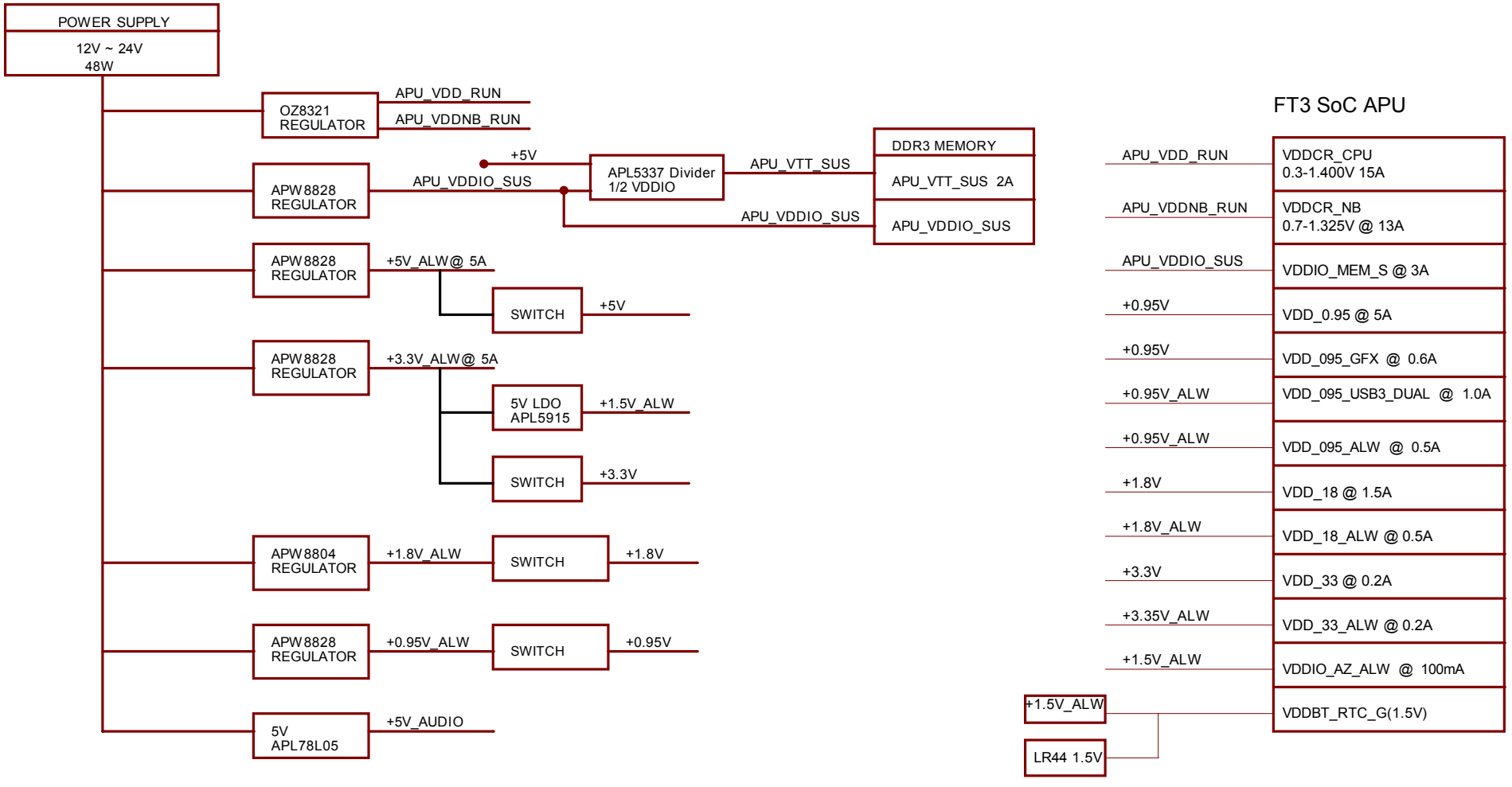

Power Distribution

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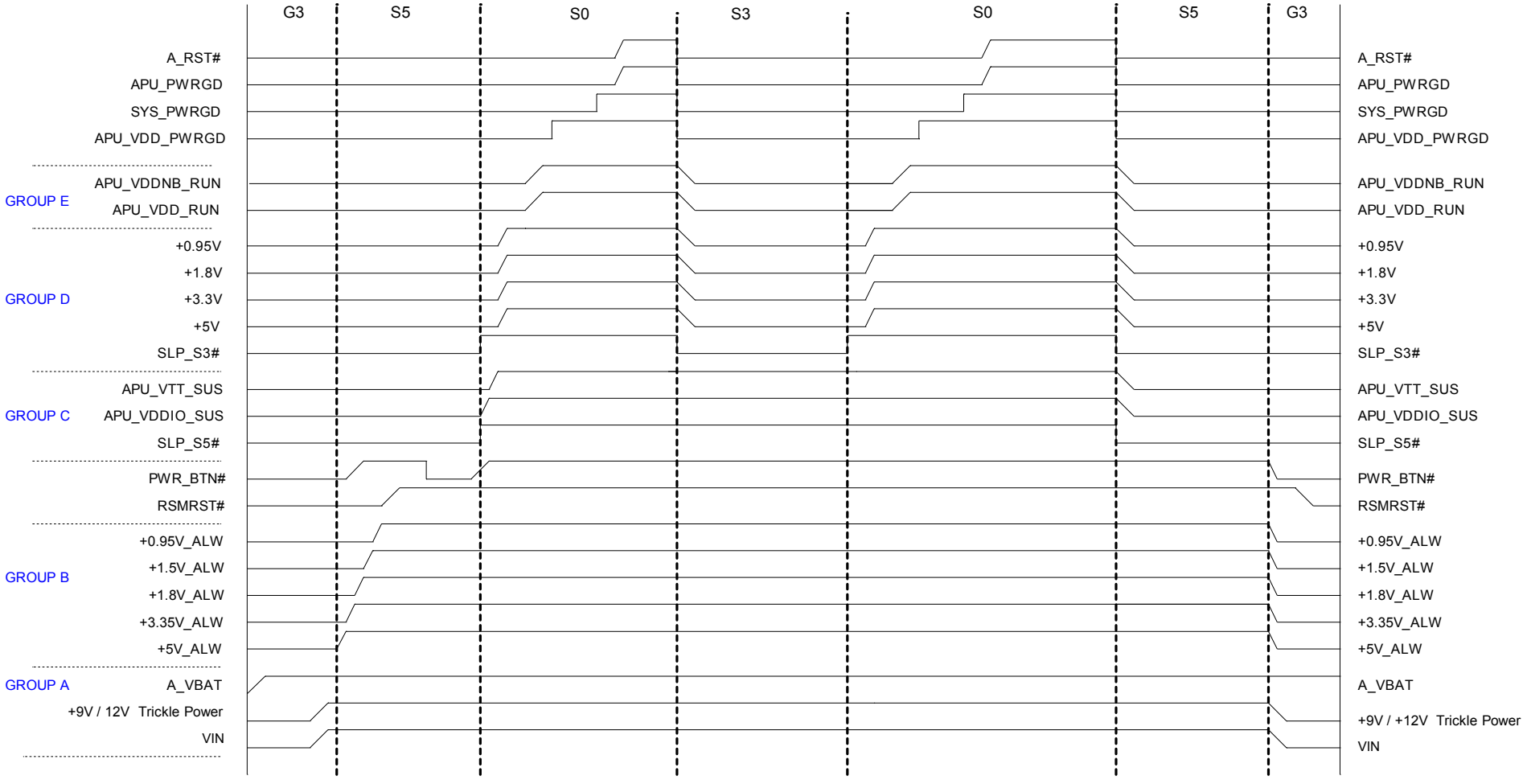
DESIGN_NOTE:
See the Electrical Data Sheet (ESD) for AMD Family 16h Models 00h-0Fh Processors (PID: 51492) for details of power sequencing.



Power Sequence Diagram

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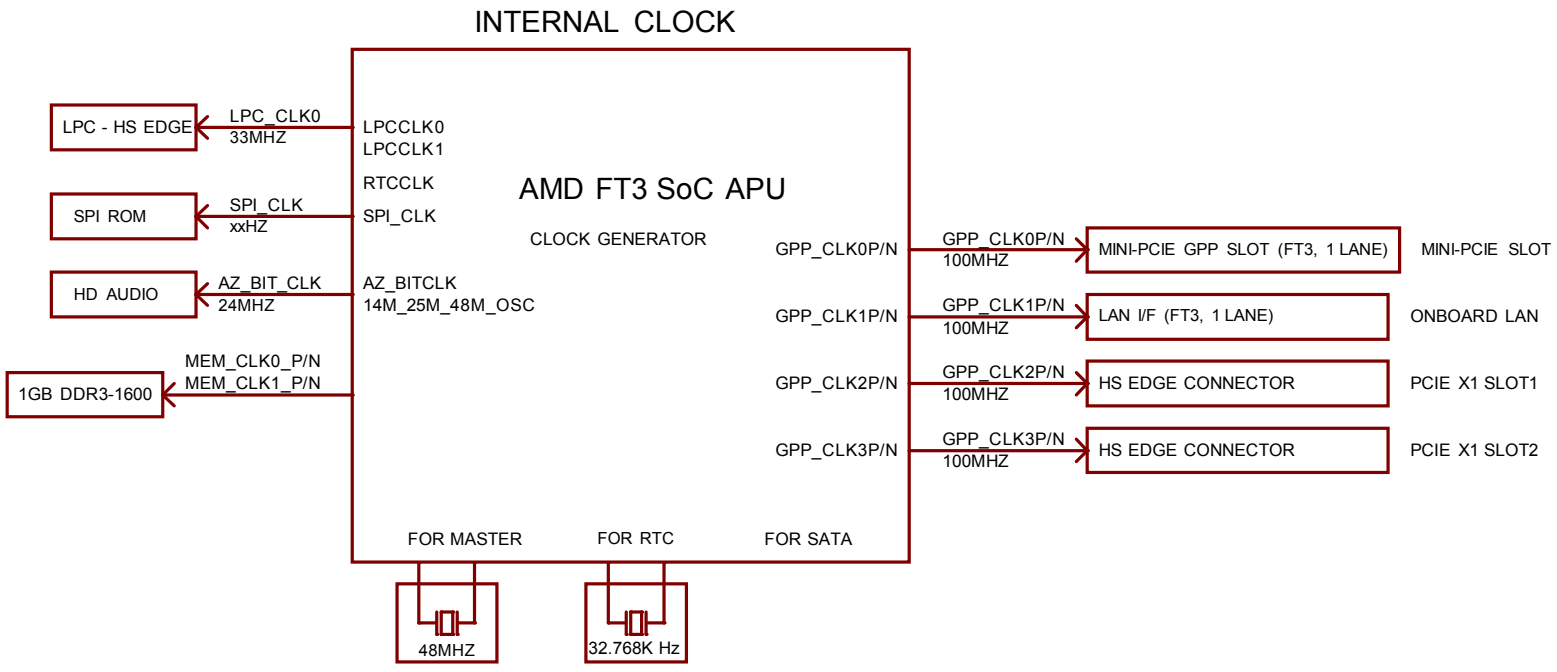

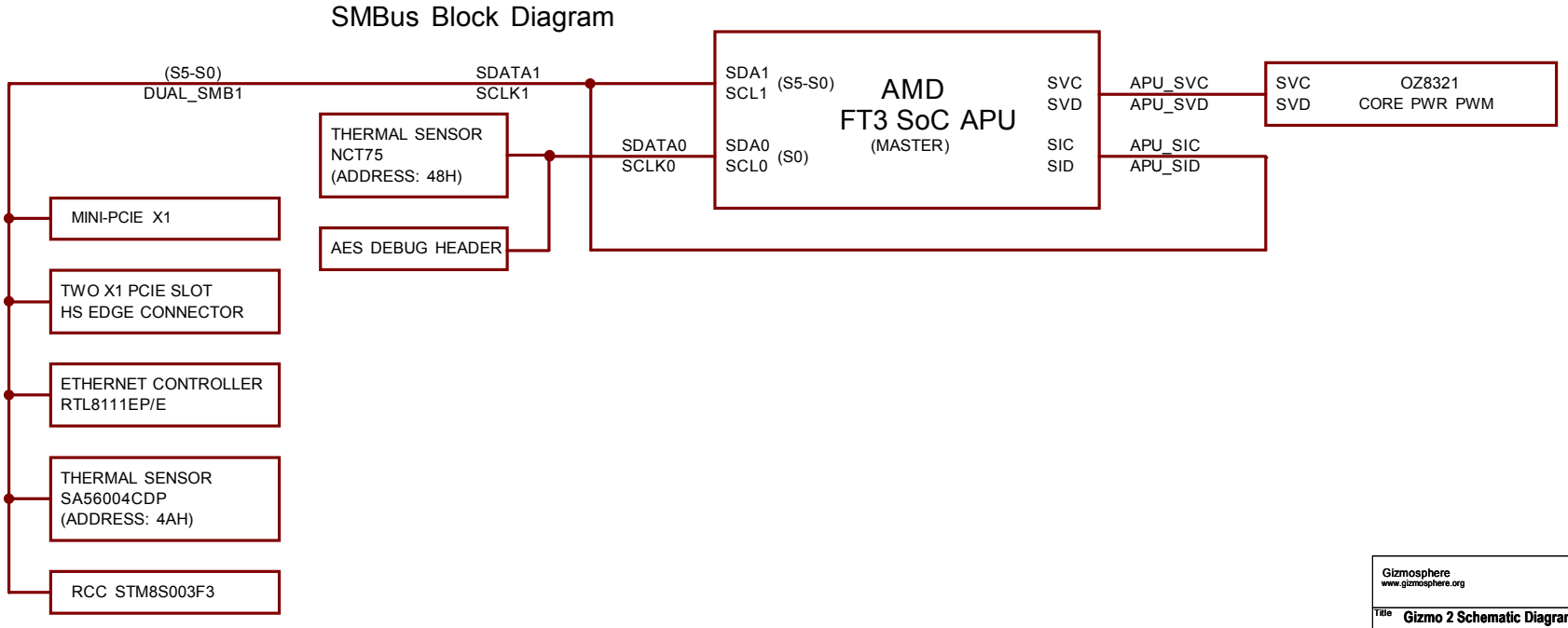

Clock Distribution/SMBus

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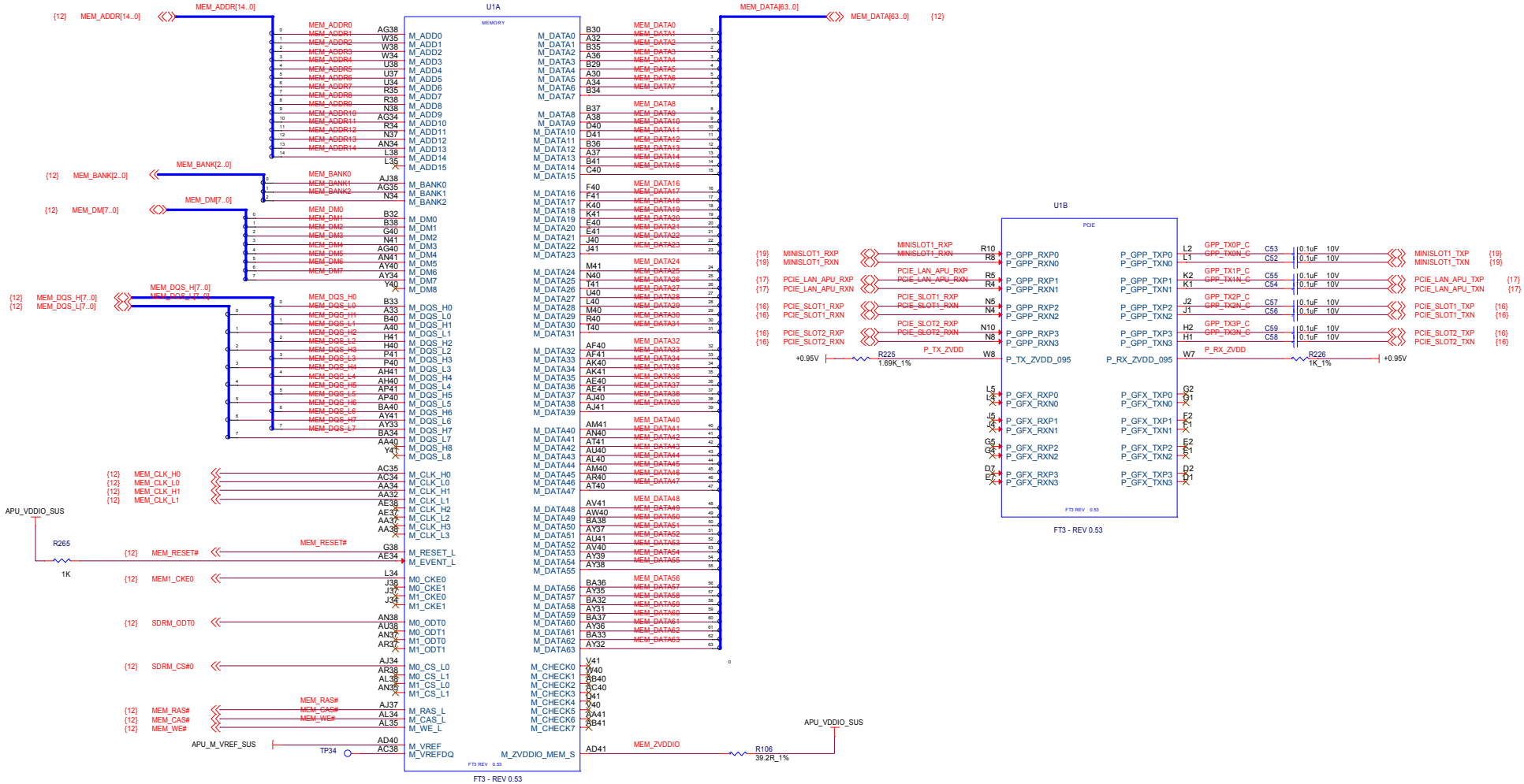

LAYOUT NOTE:
Place close to SoC APU within 1000mils of the socket.

SoC APU Memory/PCIe I/F

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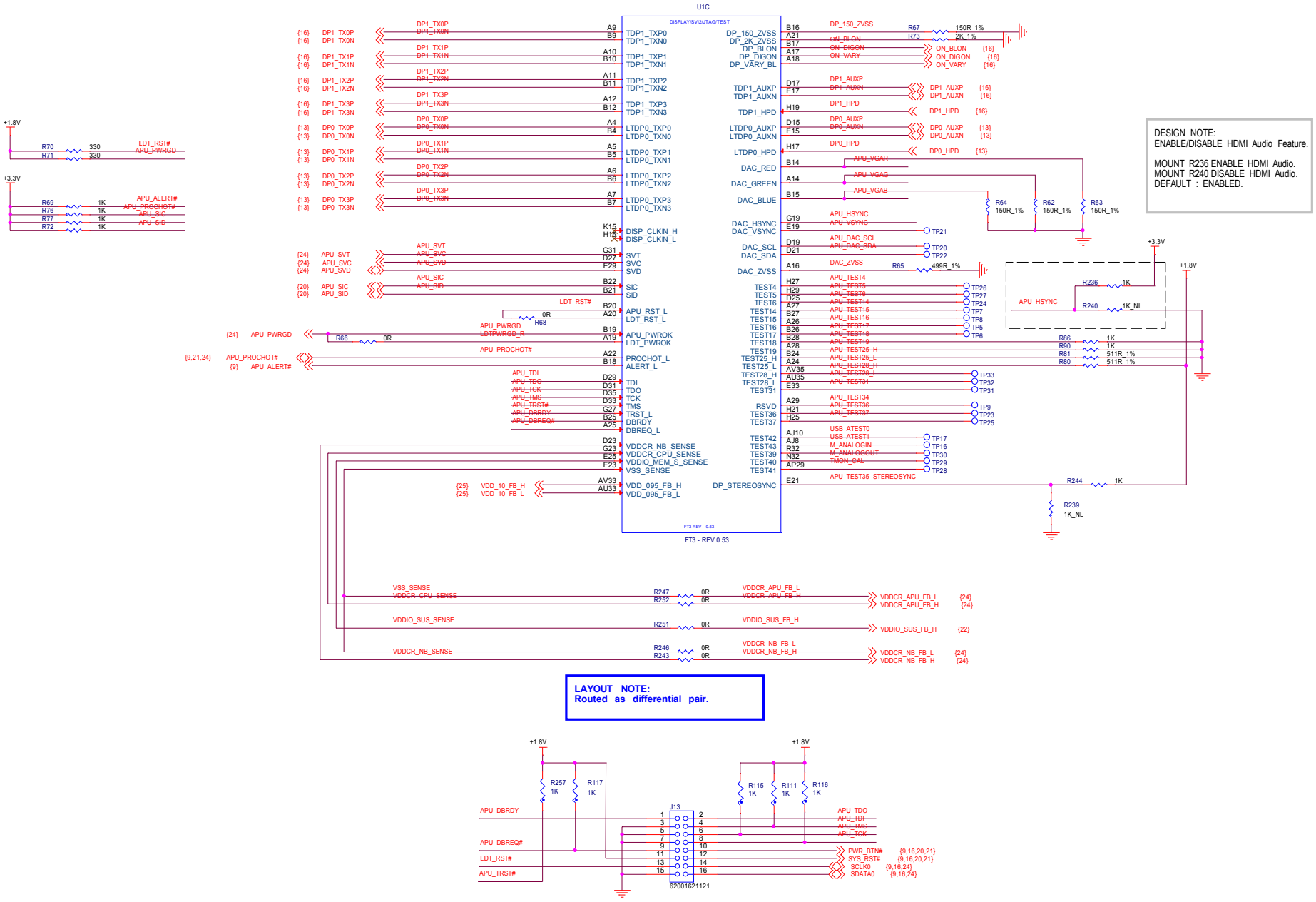

SoC APU Display/CLK/Misc.

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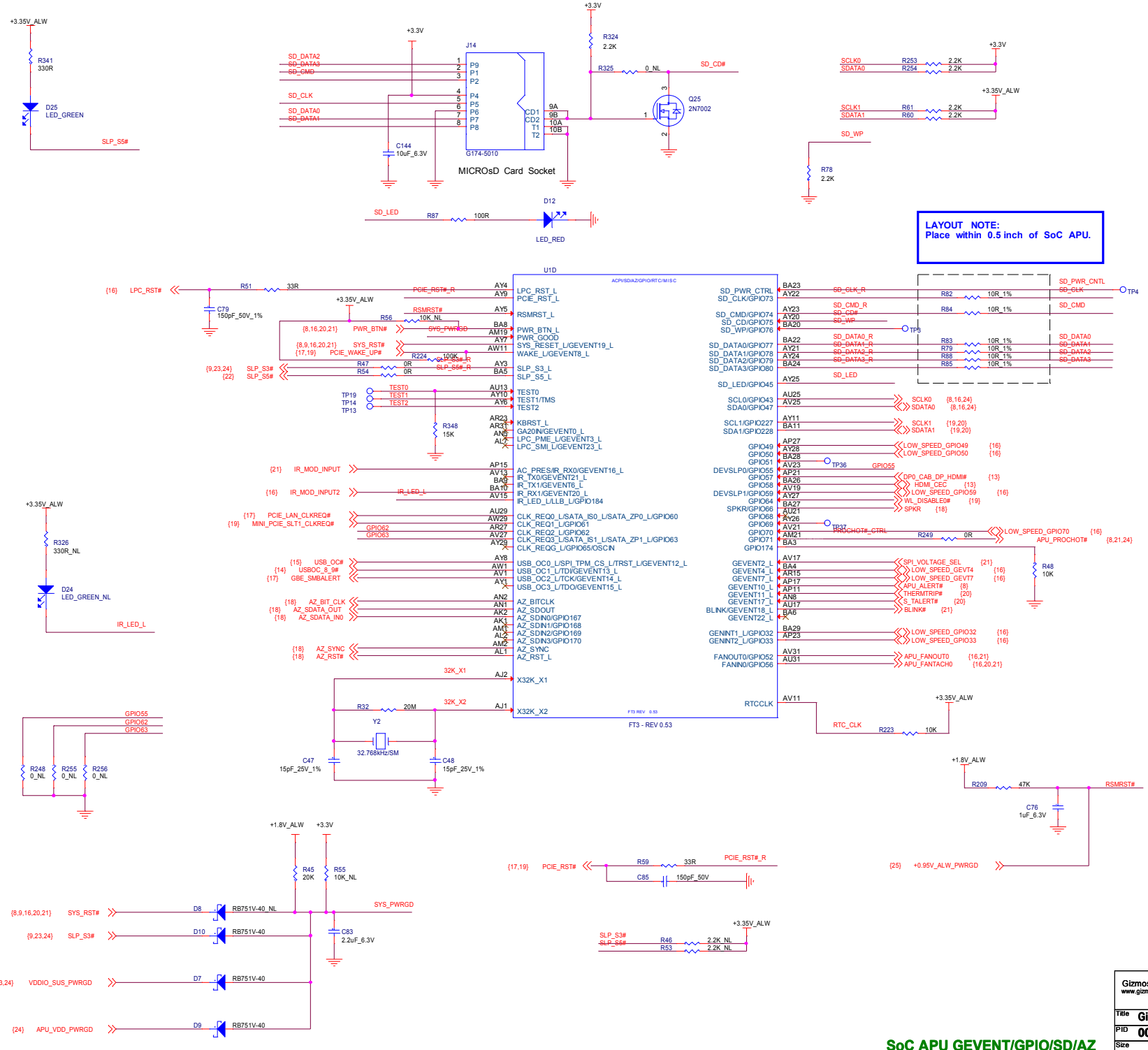
+3.35V_ALW
R341
330R
D25
LED_GREEN
SLP_S5#
+3.3V
J14
SD_DATA2
SD_DATA3
SD_CMD
SD_CLK
SD_DATA0
SD_DATA1
P9
P1
P2
P4
P5
P6
P7
P8
CD1
CD2
T1
T2
9A
9B
10A
10B
G174-5010
MICROsD Card Socket
C144
10uF_6.3V
R324
2.2K
R325
0_NL
SD_CD#
Q25
2N7002
SCLK0
SDATA0
R253
R254
2.2K
SCLK1
SDATA1
R61
R60
SD_WP
R78
2.2K
D12
SD_LED
R87
100R
LED_RED
LAYOUT NOTE:
Place within 0.5 inch of SoC APU.
U1D
ACPI/SD/AZ/GPIO/RTC/MISC
LPC_RST_L
PCIE_RST_L
RSMRST_L
PWR_BTN_L
PWR_GOOD
SYS_RESET_L/GEVENT19_L
WAKE_L/GEVENT8_L
SLP_S3_L
SLP_S5_L
TEST0
TEST1/TMS
TEST2
KBRST_L
GA20IN/GEVENT0_L
LPC_PME_L/GEVENT3_L
LPC_SMI_L/GEVENT23_L
AC_PRES/IR_RX0/GEVENT16_L
IR_TX0/GEVENT21_L
IR_TX1/GEVENT6_L
IR_RX1/GEVENT20_L
IR_LED_L/LLB_L/GPIO184
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/GPIO60
CLK_REQ1_L/GPIO61
CLK_REQ2_L/GPIO62
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/GPIO63
CLK_REQG_L/GPIO65/OSCIN
USB_OC0_L/SPI_TPM_CS_L/TRST_L/GEVENT12_L
USB_OC1_L/TDI/GEVENT13_L
USB_OC2_L/TCK/GEVENT14_L
USB_OC3_L/TDO/GEVENT15_L
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST_L
X32K_X1
X32K_X2
FT3 REV 0.53
FT3 - REV 0.53
SD_PWR_CTRL
SD_CLK/GPIO73
SD_CMD/GPIO74
SD_CD/GPIO75
SD_WP/GPIO76
SD_DATA0/GPIO77
SD_DATA1/GPIO78
SD_DATA2/GPIO79
SD_DATA3/GPIO80
SD_LED/GPIO45
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
GPIO49
GPIO50
GPIO51
DEVSLP0/GPIO55
GPIO57
GPIO58
DEVSLP1/GPIO59
GPIO64
SPKR/GPIO66
GPIO68
GPIO69
GPIO70
GPIO71
GPIO174
GEVENT2_L
GEVENT4_L
GEVENT7_L
GEVENT10_L
GEVENT11_L
GEVENT17_L
BLINK/GEVENT18_L
GEVENT22_L
GENINT1_L/GPIO32
GENINT2_L/GPIO33
FANOUT0/GPIO52
FANIN0/GPIO56
RTCCLK
SD_CLK_R
SD_CMD_R
SD_DATA0_R
SD_DATA1_R
SD_DATA2_R
SD_DATA3_R
SD_PWR_CNTL
SD_CLK
SD_CMD
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
TP4
TP5
R82
R84
R83
R79
R88
R85
10R_1%
SCLK0
SDATA0
SCLK1
SDATA1
LOW_SPEED_GPIO49
LOW_SPEED_GPIO50
TP36
GPIO55
DP0_CAB_DP_HDMI#
HDMI_CEC
LOW_SPEED_GPIO59
WL_DISABLE#
SPKR
TP37
PROCHOT#_CTRL
R249
0R
LOW_SPEED_GPIO70
APU_PROCHOT#
R48
10K
SPI_VOLTAGE_SEL
LOW_SPEED_GEVT4
LOW_SPEED_GEVT7
APU_ALERT#
THERMTRIP#
S_TALERT#
BLINK#
LOW_SPEED_GPIO32
LOW_SPEED_GPIO33
APU_FANOUT0
APU_FANTACH0
RTC_CLK
R223
10K
+3.35V_ALW
R326
330R_NL
D24
LED_GREEN_NL
IR_LED_L
GPIO55
GPIO62
GPIO63
R248
0_NL
R255
0_NL
R256
0_NL
R32
20M
Y2
32.768KHz/SM
C47
15pF_25V_1%
C48
15pF_25V_1%
C79
150pF_50V_1%
R51
33R
R56
10K_NL
R224
100K
R47
0R
R54
0R
TP19
TP14
TP13
R348
15K
R209
47K
C76
1uF_6.3V
RSMRST#
+1.8V_ALW
+3.3V
R45
20K
R55
10K_NL
D8
D10
D7
D9
RB751V-40_NL
RB751V-40
SYS_PWRGD
C83
2.2uF_6.3V
R59
33R
C85
150pF_50V
R46
R53
2.2K_NL
SoC APU GEVENT/GPIO/SD/AZ
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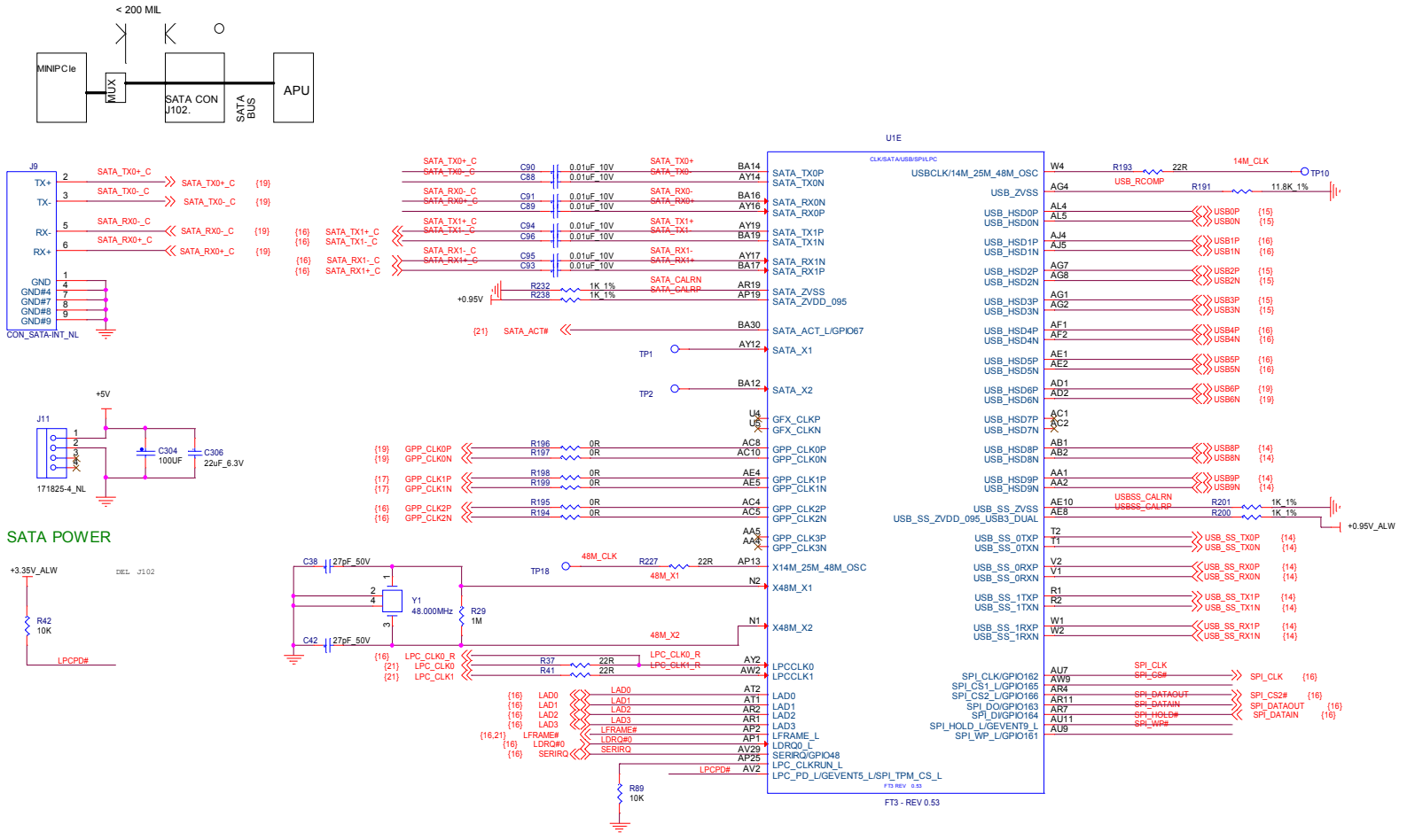
< 200 MIL
MINIPCIe
MUX
SATA CON
U102.
SATA
BUS
APU
U1E
CLK/SATA/USB/SPI/LPC
SATA_TX0P
SATA_TX0N
SATA_RX0N
SATA_RX0P
SATA_TX1P
SATA_TX1N
SATA_RX1N
SATA_RX1P
SATA_ZVSS
SATA_ZVDD_095
SATA_ACT_L/GPIO67
SATA_X1
SATA_X2
GFX_CLKP
GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
X14M_25M_48M_OSC
X48M_X1
X48M_X2
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME_L
LDRQ0_L
SERIRQ/GPIO48
LPC_CLKRUN_L
LPC_PD_L/GEVENT5_L/SPI_TPM_CS_L
USBCLK/14M_25M_48M_OSC
USB_ZVSS
USB_HSD0P
USB_HSD0N
USB_HSD1P
USB_HSD1N
USB_HSD2P
USB_HSD2N
USB_HSD3P
USB_HSD3N
USB_HSD4P
USB_HSD4N
USB_HSD5P
USB_HSD5N
USB_HSD6P
USB_HSD6N
USB_HSD7P
USB_HSD7N
USB_HSD8P
USB_HSD8N
USB_HSD9P
USB_HSD9N
USB_SS_ZVSS
USB_SS_ZVDD_095_USB3_DUAL
USB_SS_0TXP
USB_SS_0TXN
USB_SS_0RXP
USB_SS_0RXN
USB_SS_1TXP
USB_SS_1TXN
USB_SS_1RXP
USB_SS_1RXN
SPI_CLK/GPIO162
SPI_CS1_L/GPIO165
SPI_CS2_L/GPIO166
SPI_DO/GPIO163
SPI_DI/GPIO164
SPI_HOLD_L/GEVENT9_L
SPI_WP_L/GPIO161
FT3 REV 0.53
FT3 - REV 0.53
J9
CON_SATA-INT_NL
J11
171825-4_NL
SATA POWER
+5V
+3.35V_ALW
+0.95V
+0.95V_ALW
DEL J102
DEL D103.
D11
RB751S40H
3.3V_SPI
U4
MX25L3236DM2I-10
J12
HEADER_2X4
FOR SPI PROGRAMMER
SoC APU SATA/USB/SPI/CLK
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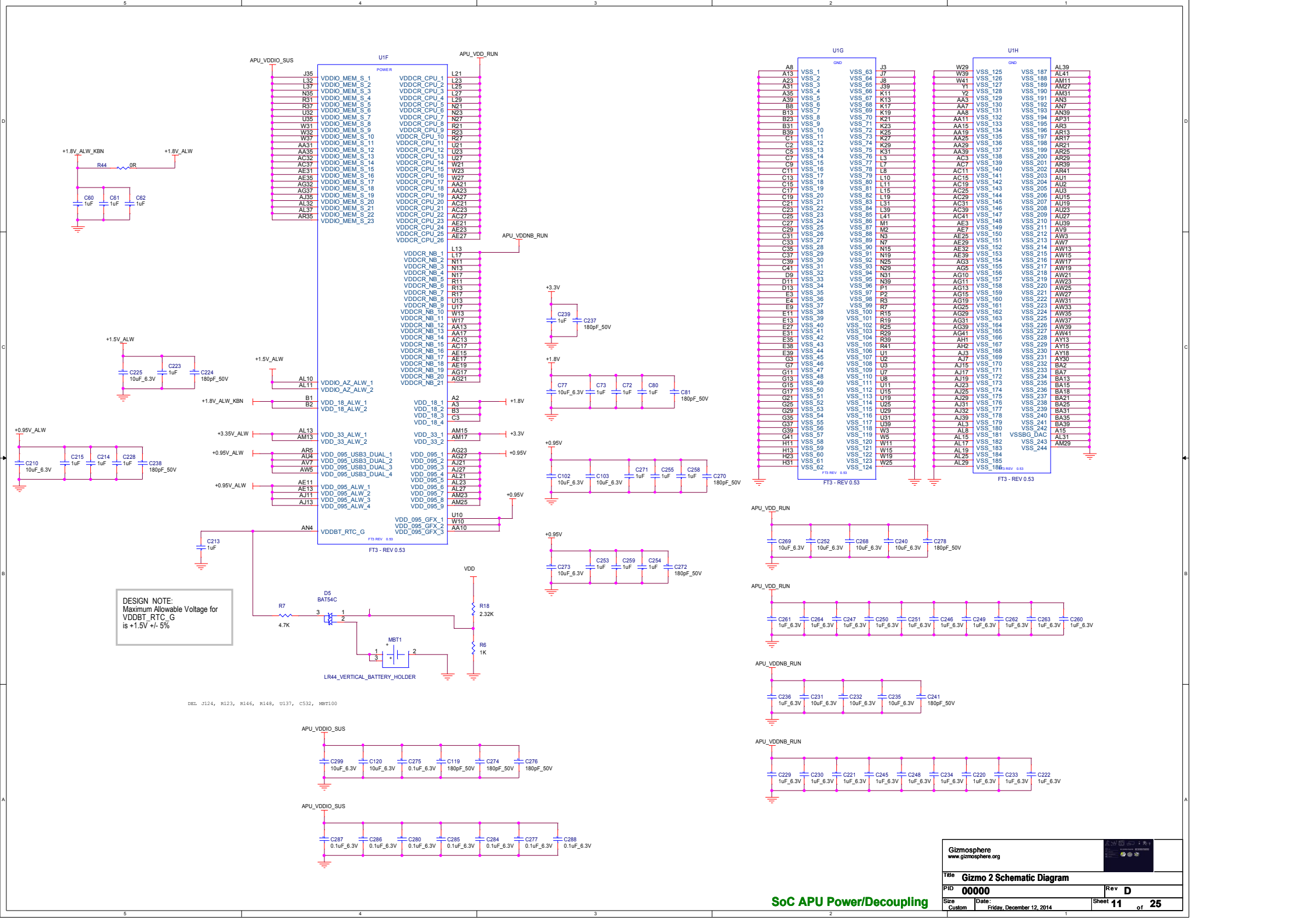
U1F
POWER
APU_VDDIO_SUS
APU_VDD_RUN
APU_VDDNB_RUN
+1.8V_ALW_KBN
+1.8V_ALW
R44
0R
C60 1uF
C61 1uF
C62 1uF
+1.5V_ALW
C225 10uF_6.3V
C223 1uF
C224 180pF_50V
+0.95V_ALW
C210 10uF_6.3V
C215 1uF
C214 1uF
C228 1uF
C238 180pF_50V
+3.35V_ALW
C213 1uF
+1.8V
+3.3V
+0.95V
VDD
DESIGN NOTE:
Maximum Allowable Voltage for
VDDBT_RTC_G
is +1.5V +/- 5%
D5
BAT54C
R7
4.7K
R18
2.32K
R6
1K
MBT1
LR44_VERTICAL_BATTERY_HOLDER
FT3 - REV 0.53
DEL J124, R123, R146, R148, U137, C532, MBT100
U1G
U1H
GND
FT3 - REV 0.53
C239 1uF
C237 180pF_50V
C77 10uF_6.3V
C73 1uF
C72 1uF
C80 1uF
C81 180pF_50V
C102 10uF_6.3V
C103 10uF_6.3V
C271 1uF
C255 1uF
C258 1uF
C270 180pF_50V
C273 10uF_6.3V
C253 1uF
C259 1uF
C254 1uF
C272 180pF_50V
C269 10uF_6.3V
C252 10uF_6.3V
C268 10uF_6.3V
C240 10uF_6.3V
C278 180pF_50V
C261 1uF_6.3V
C264 1uF_6.3V
C247 1uF_6.3V
C250 1uF_6.3V
C251 1uF_6.3V
C246 1uF_6.3V
C249 1uF_6.3V
C262 1uF_6.3V
C263 1uF_6.3V
C260 1uF_6.3V
C236 1uF_6.3V
C231 10uF_6.3V
C232 10uF_6.3V
C235 10uF_6.3V
C241 180pF_50V
C229 1uF_6.3V
C230 1uF_6.3V
C221 1uF_6.3V
C245 1uF_6.3V
C248 1uF_6.3V
C234 1uF_6.3V
C220 1uF_6.3V
C233 1uF_6.3V
C222 1uF_6.3V
C299 10uF_6.3V
C120 10uF_6.3V
C275 0.1uF_6.3V
C119 180pF_50V
C274 180pF_50V
C276 180pF_50V
C287 0.1uF_6.3V
C286 0.1uF_6.3V
C280 0.1uF_6.3V
C285 0.1uF_6.3V
C284 0.1uF_6.3V
C277 0.1uF_6.3V
C288 0.1uF_6.3V
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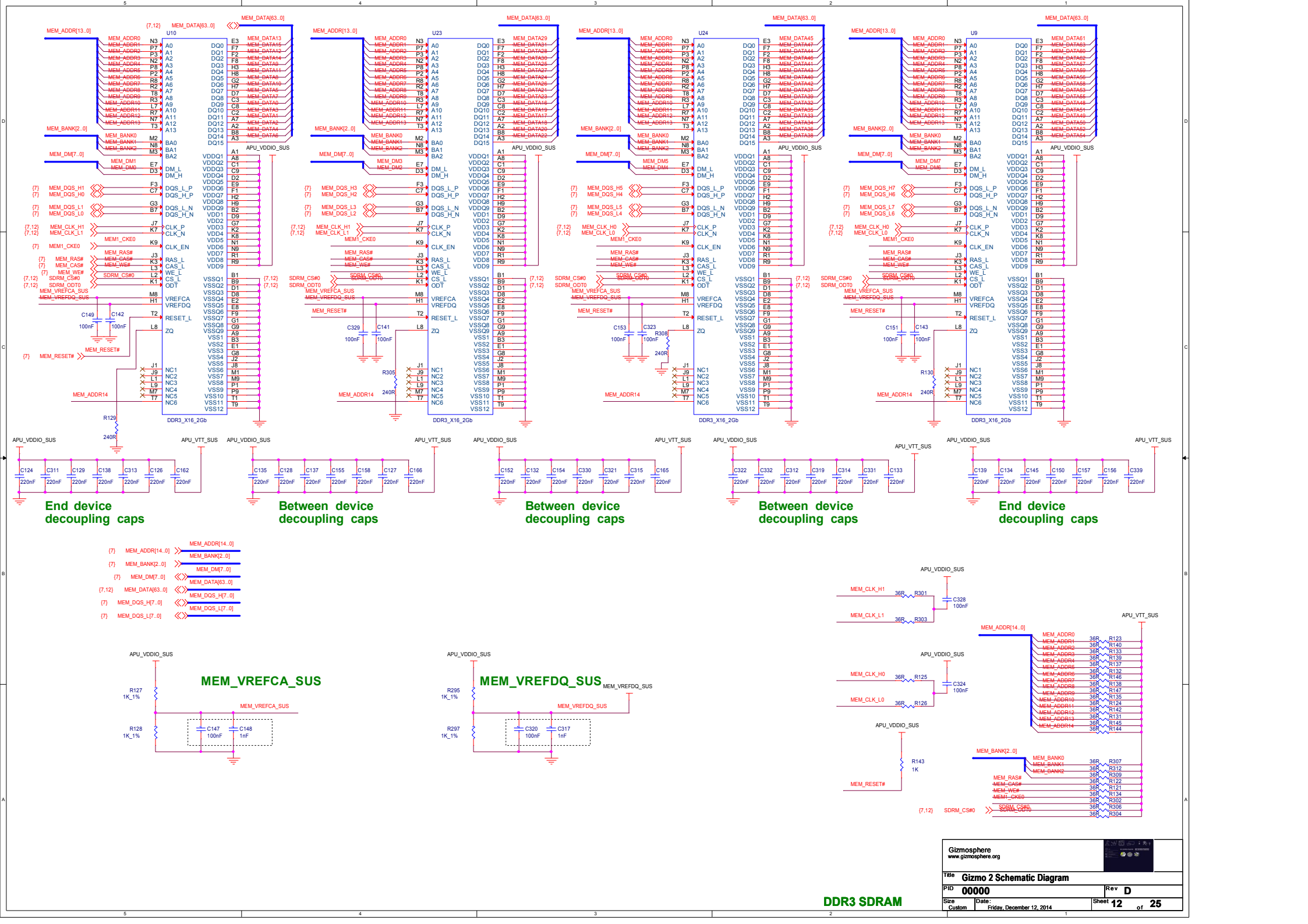
SoC APU Power/Decoupling


U10
U23
U24
U9
DDR3_X16_2Gb
APU_VDDIO_SUS
APU_VTT_SUS
End device decoupling caps
Between device decoupling caps
Between device decoupling caps
Between device decoupling caps
End device decoupling caps
MEM_VREFCA_SUS
MEM_VREFDQ_SUS
DDR3 SDRAM
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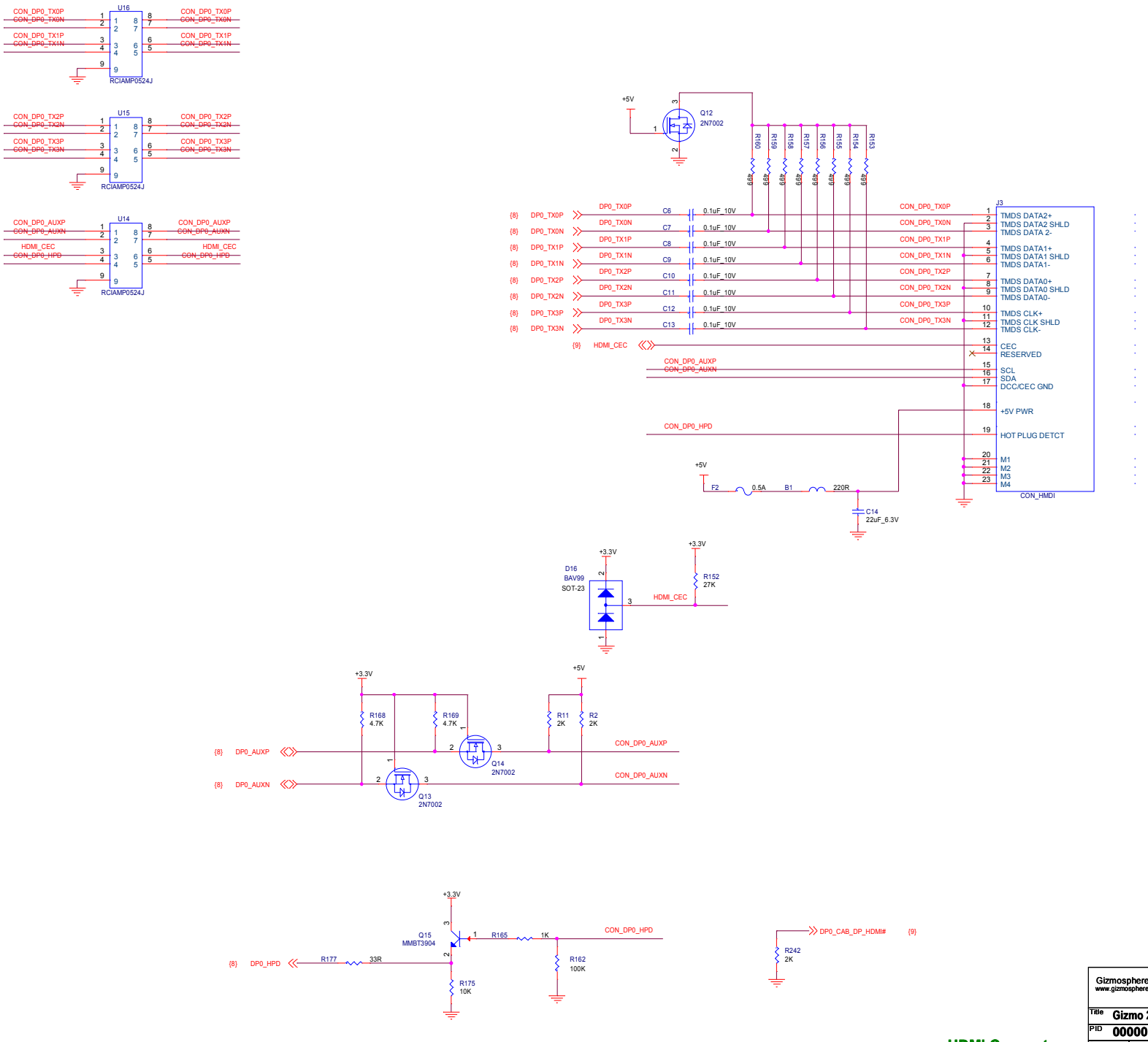

HDMI Connector

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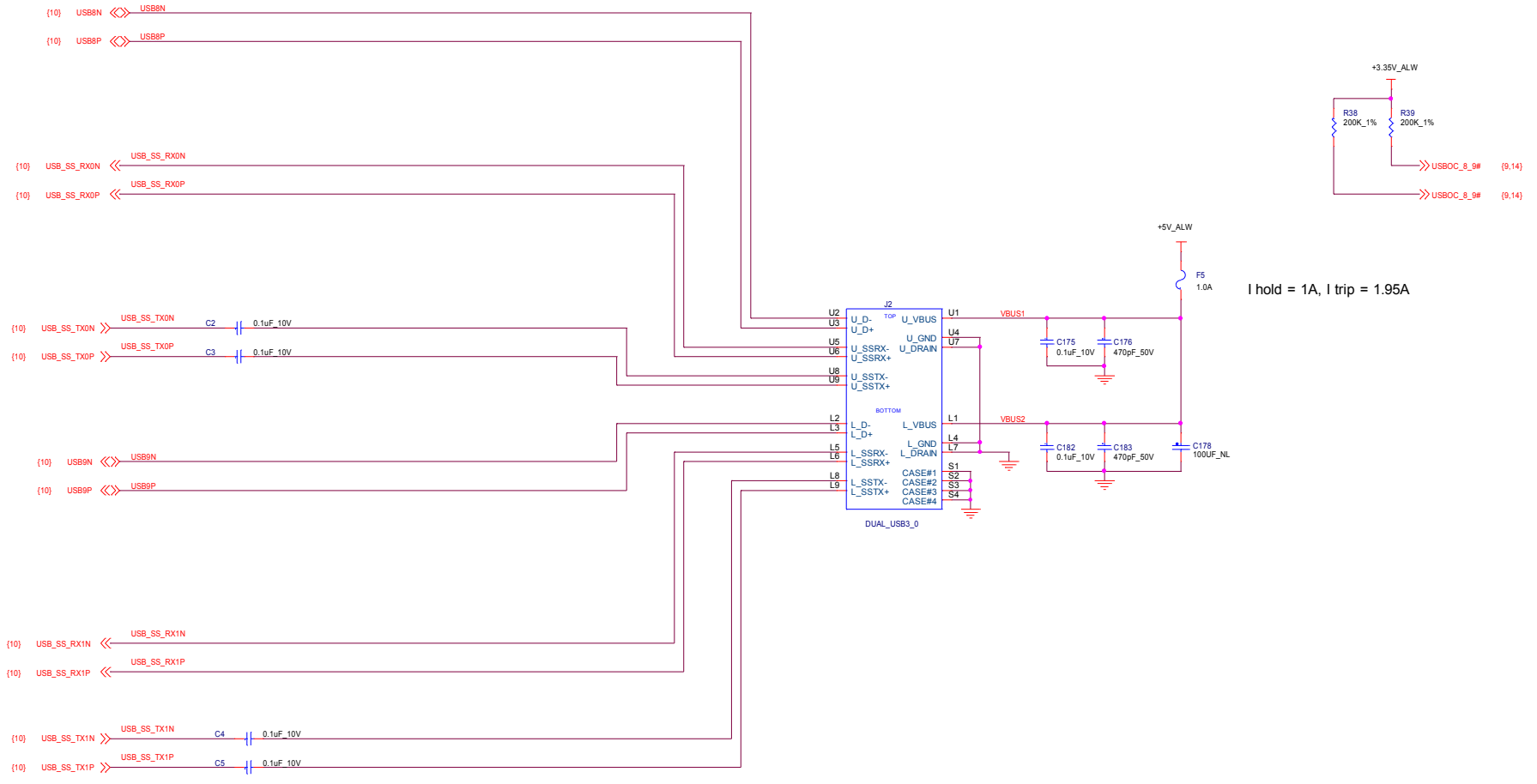

USB 3.0 Port x2

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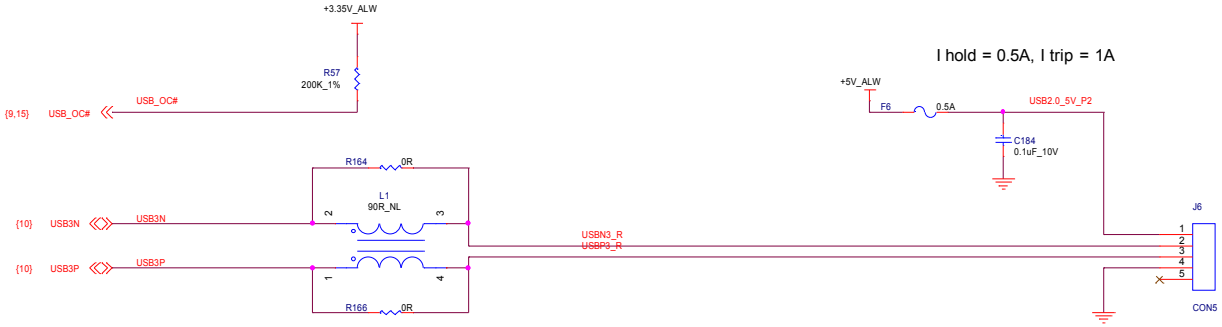

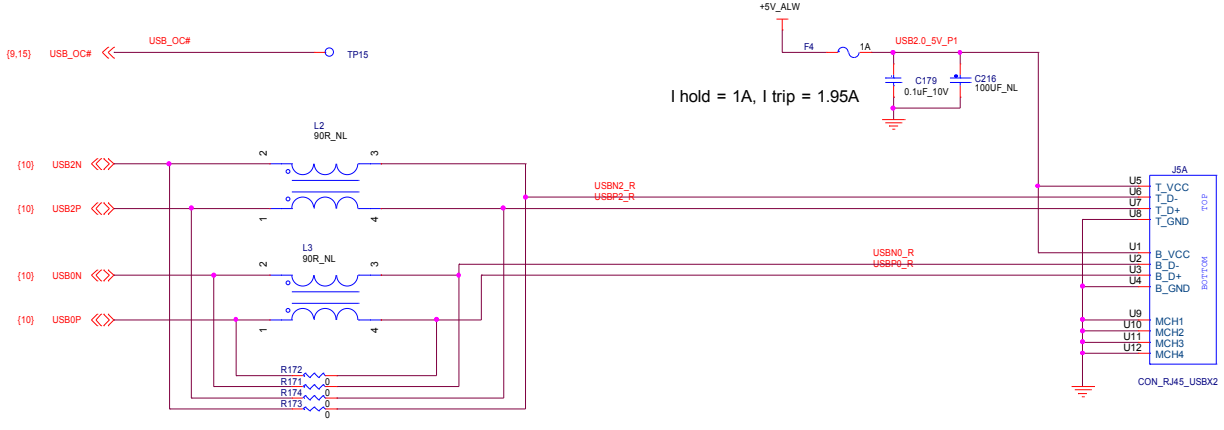

USB 2.0 HEADER & USB-TYPE A (x4 Port)

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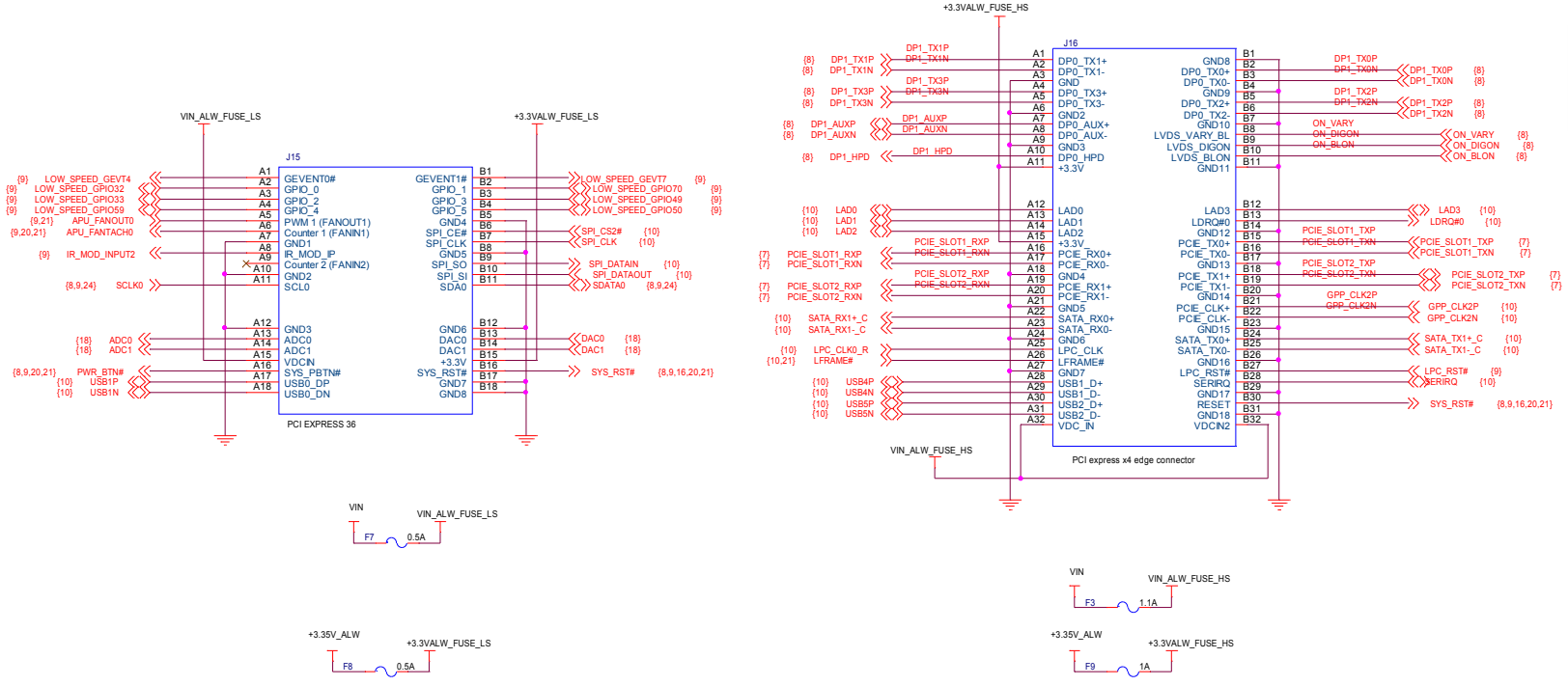

DESIGN NOTE:
PCIe lanes can be independent and connected to two different devices; or ganged and connected to a single device.

DESIGN NOTE:
This SATA port supports port multiplier devices allowing for multiple SATA drives connected to this single port.

LOW SPEED EDGE CONNECTOR

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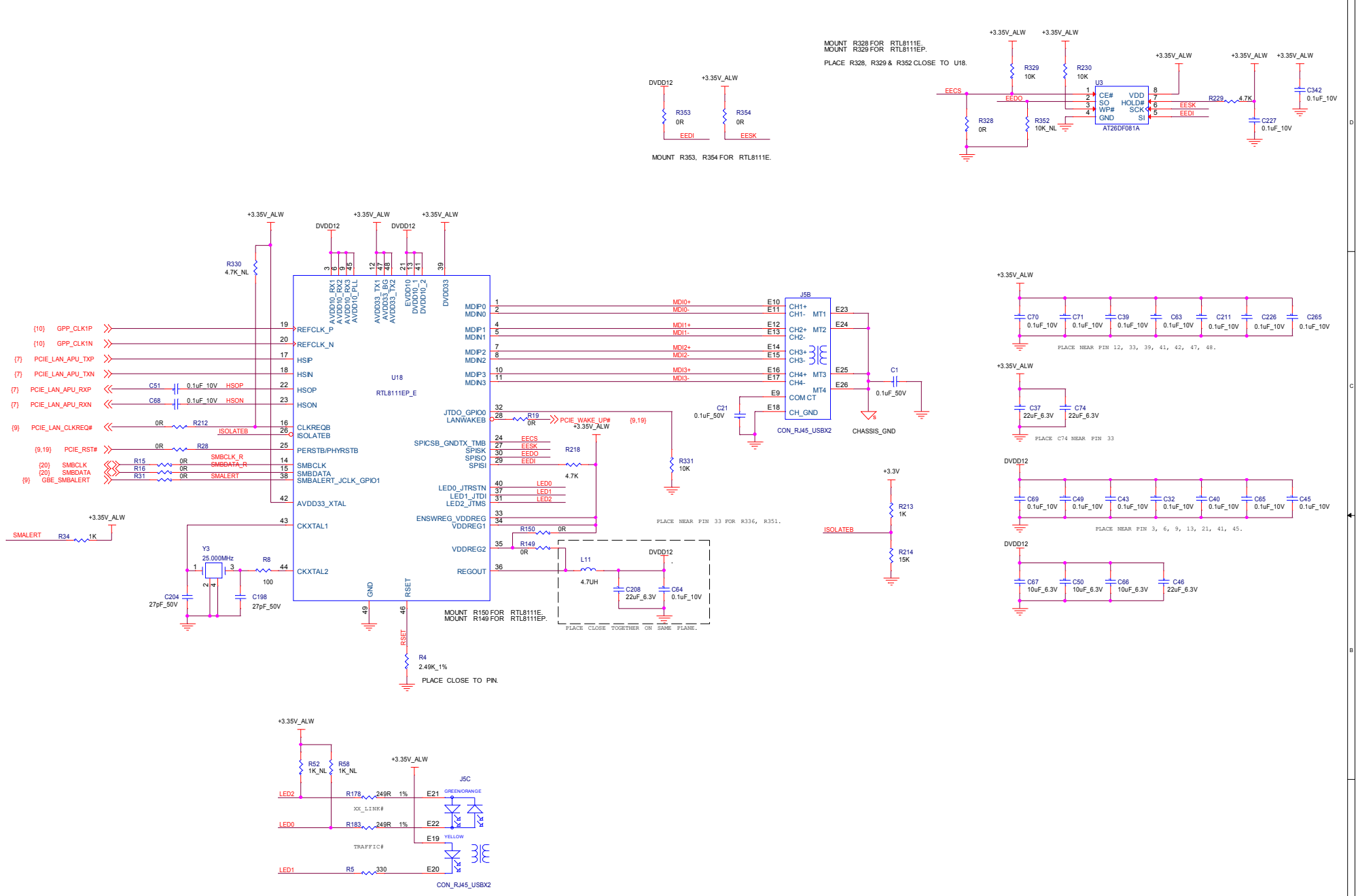
MOUNT R328 FOR RTL8111E.
MOUNT R329 FOR RTL8111EP.
PLACE R328, R329 & R352 CLOSE TO U18.
+3.35V_ALW
R329 10K
R230 10K
U3
CE# VDD
SO HOLD#
WP# SCK
GND SI
AT26DF081A
EECS
EEDO
EESK
EEDI
R328 0R
R352 10K_NL
R229 4.7K
C227 0.1uF_10V
C342 0.1uF_10V
DVDD12
R353 0R
R354 0R
MOUNT R353, R354 FOR RTL8111E.
U18
RTL8111EP_E
REFCLK_P
REFCLK_N
HSIP
HSIN
HSOP
HSON
CLKREQB
ISOLATEB
PERSTB/PHYRSTB
SMBCLK
SMBDATA
SMBALERT_JCLK_GPIO1
AVDD33_XTAL
CKXTAL1
CKXTAL2
RSET
R4 2.49K_1%
PLACE CLOSE TO PIN.
MDIP0 MDIN0
MDIP1 MDIN1
MDIP2 MDIN2
MDIP3 MDIN3
JTDO_GPIO0
LANWAKEB
SPICSB_GNDTX_TMB
SPISK
SPISO
SPISI
LED0_JTRSTN
LED1_JTDI
LED2_JTMS
ENSWREG_VDDREG
VDDREG1
VDDREG2
REGOUT
PCIE_WAKE_UP#
R331 10K
R218 4.7K
L11 4.7UH
R150 0R
R149 0R
MOUNT R150 FOR RTL8111E.
MOUNT R149 FOR RTL8111EP.
PLACE CLOSE TOGETHER ON SAME PLANE.
PLACE NEAR PIN 33 FOR R336, R351.
J5B
CON_RJ45_USBX2
CHASSIS_GND
C1 0.1uF_50V
C21 0.1uF_50V
GPP_CLK1P
GPP_CLK1N
PCIE_LAN_APU_TXP
PCIE_LAN_APU_TXN
PCIE_LAN_APU_RXP
PCIE_LAN_APU_RXN
PCIE_LAN_CLKREQ#
PCIE_RST#
SMBCLK
SMBDATA
GBE_SMBALERT
SMBCLK_R
SMBDATA_R
SMALERT
C51 0.1uF_10V HSOP
C68 0.1uF_10V HSON
R212 0R ISOLATEB
R28 0R
R15 0R
R16 0R
R31 0R
R34 1K
Y3 25.000MHz
R8 100
C204 27pF_50V
C198 27pF_50V
C208 22uF_6.3V
C64 0.1uF_10V
R330 4.7K_NL
R213 1K
R214 15K
C70 0.1uF_10V
C71 0.1uF_10V
C39 0.1uF_10V
C63 0.1uF_10V
C211 0.1uF_10V
C226 0.1uF_10V
C265 0.1uF_10V
PLACE NEAR PIN 12, 33, 39, 41, 42, 47, 48.
C37 22uF_6.3V
C74 22uF_6.3V
PLACE C74 NEAR PIN 33
C69 0.1uF_10V
C49 0.1uF_10V
C43 0.1uF_10V
C32 0.1uF_10V
C40 0.1uF_10V
C65 0.1uF_10V
C45 0.1uF_10V
PLACE NEAR PIN 3, 6, 9, 13, 21, 41, 45.
C67 10uF_6.3V
C50 10uF_6.3V
C66 10uF_6.3V
C46 22uF_6.3V
R52 1K_NL
R58 1K_NL
J5C
LED2
LED0
LED1
R178 249R 1%
R183 249R 1%
R5 330
XX_LINK#
TRAFFIC#
GREEN/ORANGE
YELLOW
CON_RJ45_USBX2
SET OFFSET REG 0x18 : 0x0482
USE RTNICPG V2.44 OR HIGHER.
Gigabit Ethernet w/DASH
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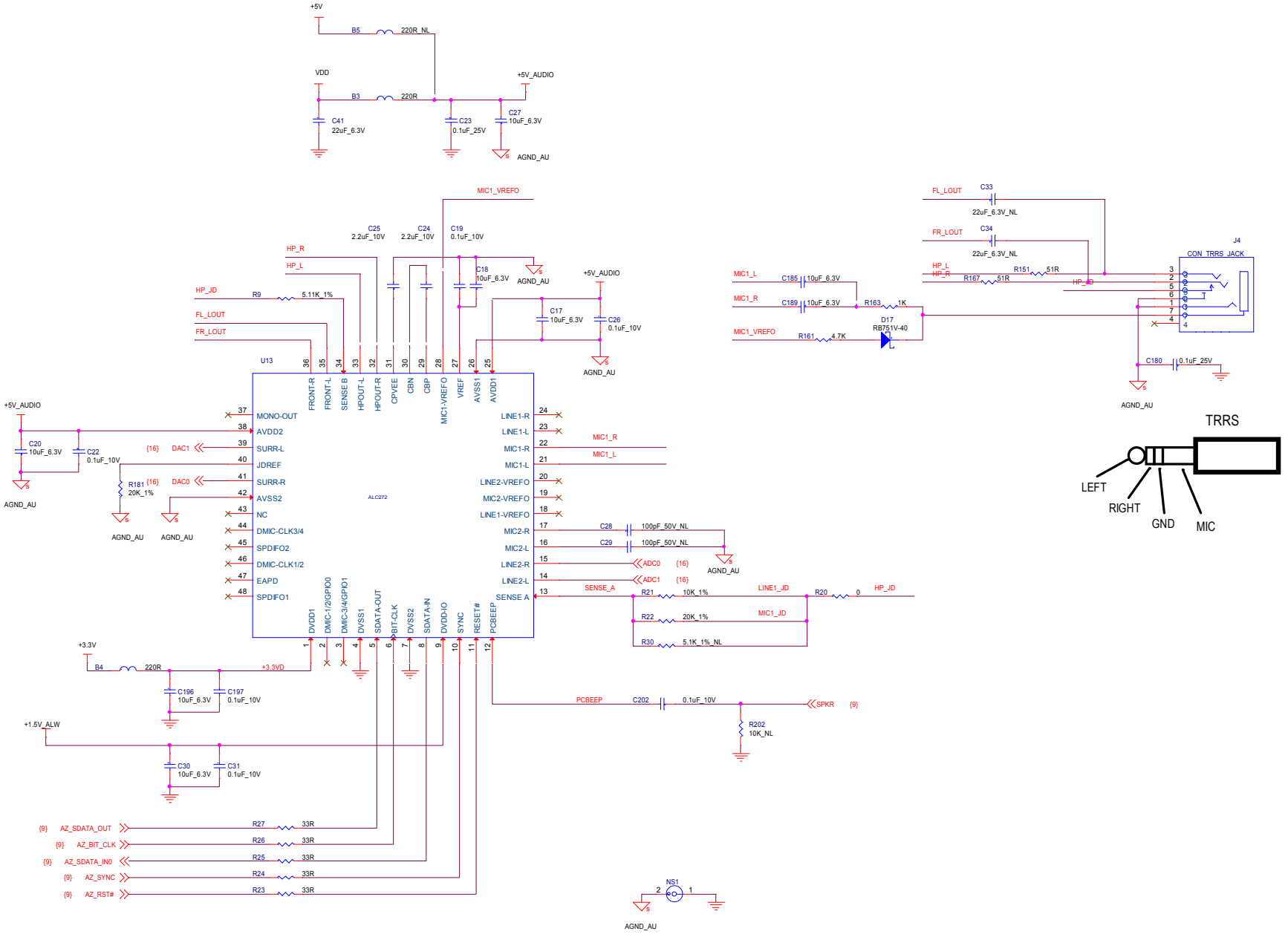
DESIGN NOTE:
Regulator is optional for better quality analog audio,
ALC272 can be connected directly to +5V.



HD Audio Codec

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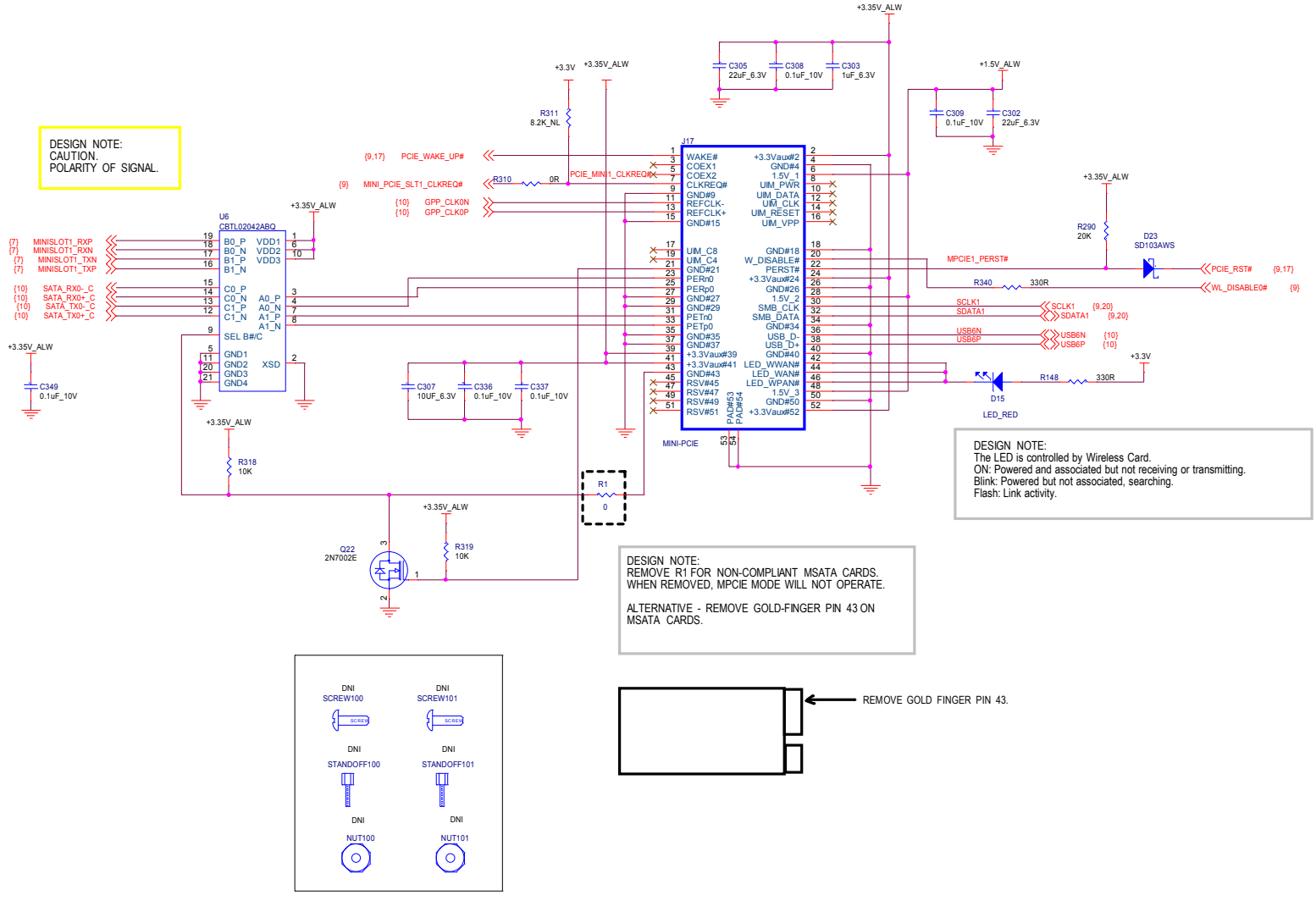

Mini-PCIe Slot

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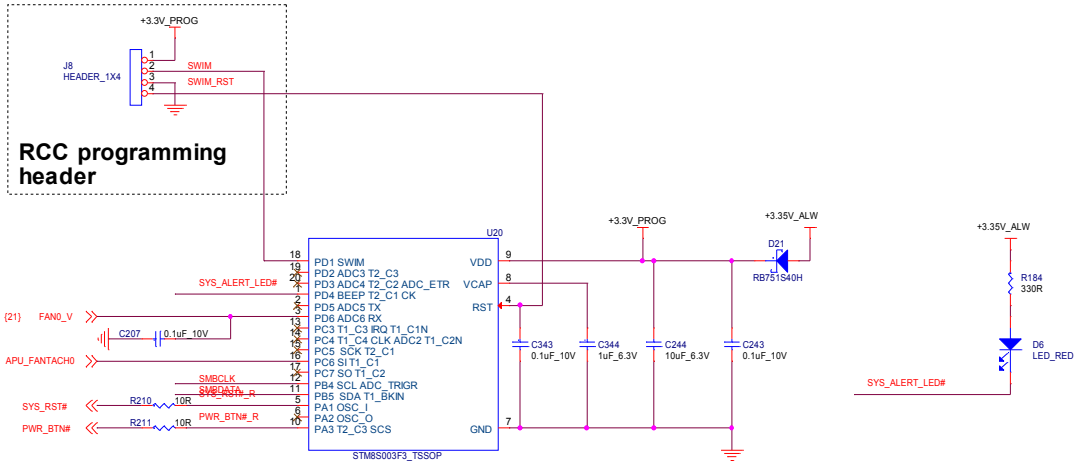

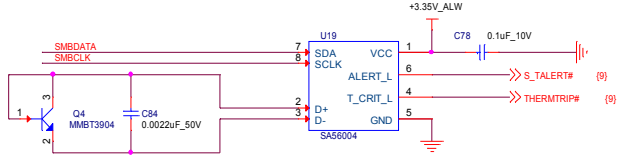

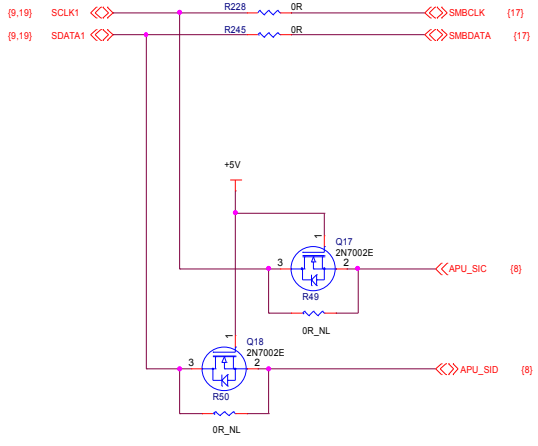

DASH/RCC

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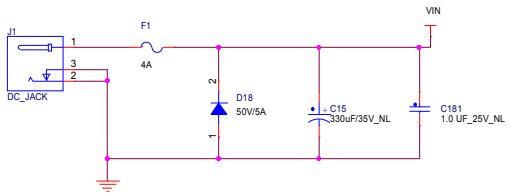
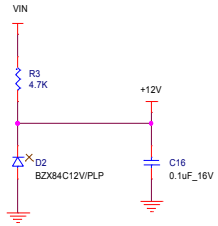
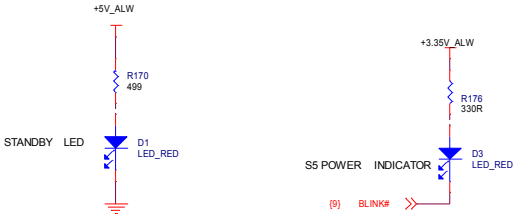
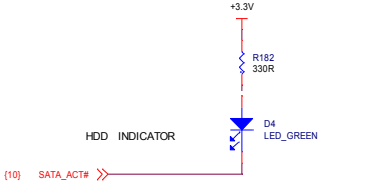
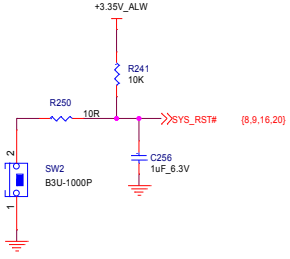




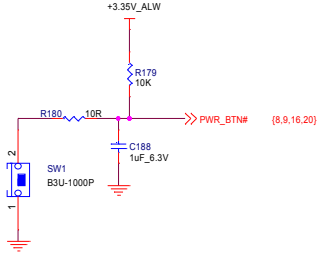
+12V TRICKLE POWER



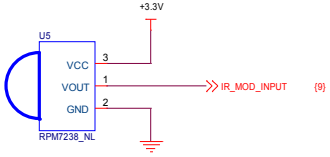




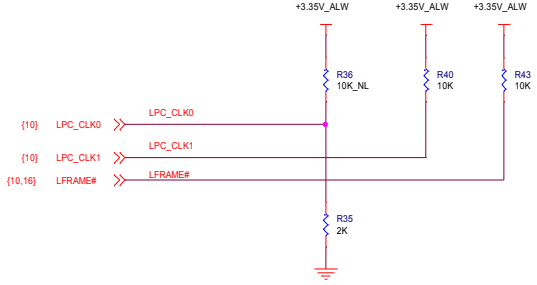
RESET BUTTON

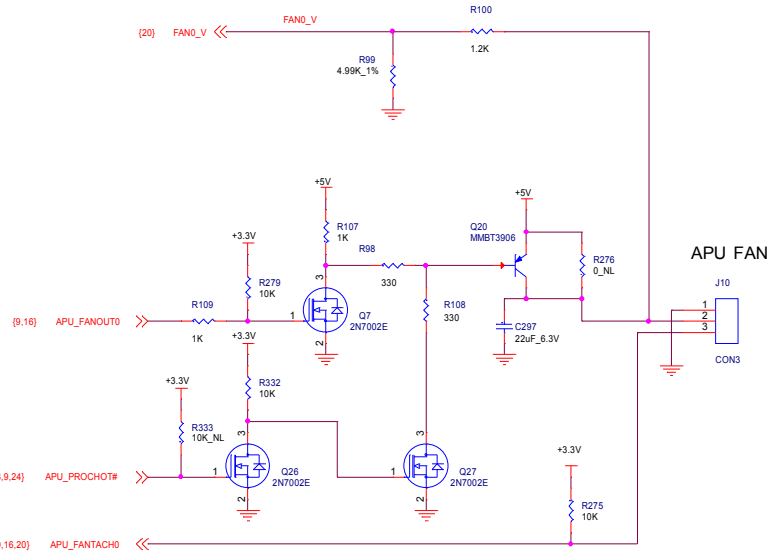


POWER BUTTON

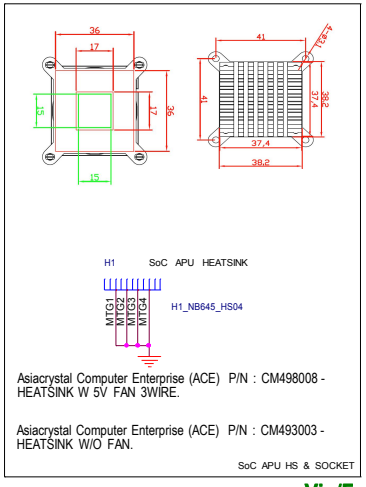


DESIGN:
The LED is controlled by SoC APU BLINK or another GPIO pin:
On: S0 state.
Blink: S3 state.





APU FAN

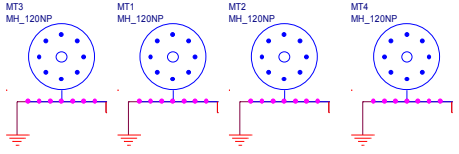


Asiacrystal Computer Enterprise (ACE) P/N : CM498008 - HEATSINK W 5V FAN 3WIRE.

Asiacrystal Computer Enterprise (ACE) P/N : CM493003 - HEATSINK W/O FAN.

SoC APU HS & SOCKET

	LPC_CLK0	LPC_CLK1	LFRAME#	SPI_BOLTAGE_SEL
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED (DEFAULT)	SPI ROM (DEFAULT)	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM (DEFAULT)



Vin/Fan/LEDs/PowerUp Scrap.

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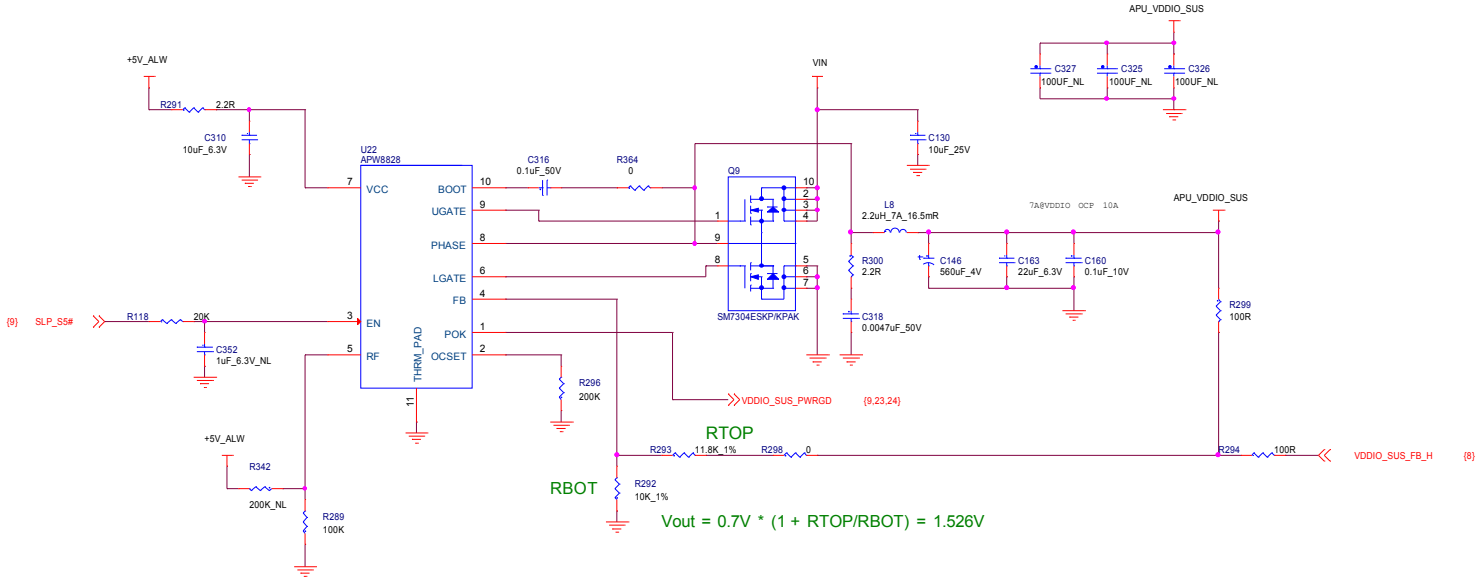

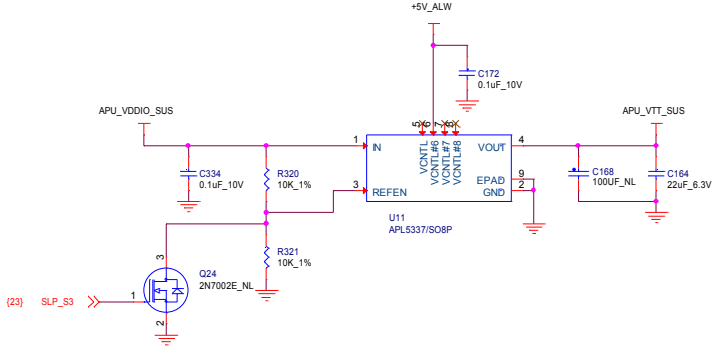

Dual Power/VDDIO_SUS

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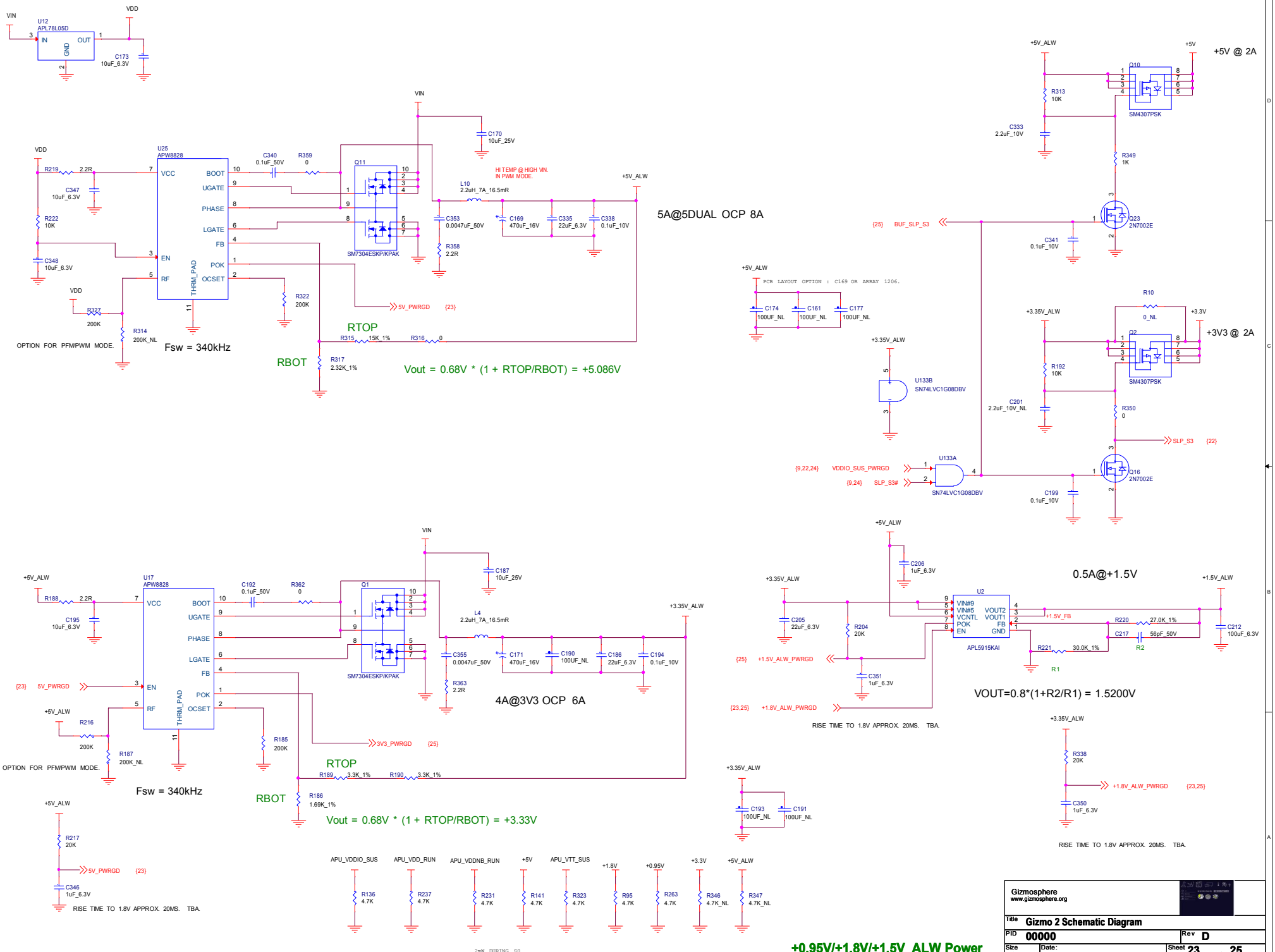
VIN
U12
APL78L05D
IN
OUT
GND
VDD
C173
10uF_6.3V
U25
APW8828
VCC
BOOT
UGATE
PHASE
LGATE
FB
POK
OCSET
EN
RF
THRM_PAD
R219
2.2R
C347
10uF_6.3V
R222
10K
C348
10uF_6.3V
R227
200K
R314
200K_NL
OPTION FOR PFM/PWM MODE.
Fsw = 340kHz
C340
0.1uF_50V
R359
0
Q11
SM7304ESKP/KPAK
C170
10uF_25V
HI TEMP @ HIGH VIN.
IN PWM MODE.
L10
2.2uH_7A_16.5mR
C353
0.0047uF_50V
C169
470uF_16V
C335
22uF_6.3V
C338
0.1uF_10V
R358
2.2R
+5V_ALW
5A@5DUAL OCP 8A
5V_PWRGD
{23}
R322
200K
RTOP
R315
15K_1%
R316
0
RBOT
R317
2.32K_1%
Vout = 0.68V * (1 + RTOP/RBOT) = +5.086V
+5V_ALW
+5V
+5V @ 2A
R313
10K
C333
2.2uF_10V
Q10
SM4307PSK
R349
1K
Q23
2N7002E
{25}
BUF_SLP_S3
C341
0.1uF_10V
PCB LAYOUT OPTION : C169 OR ARRAY 1206.
C174
100UF_NL
C161
100UF_NL
C177
100UF_NL
+3.35V_ALW
U133B
SN74LVC1G08DBV
R10
0_NL
+3.3V
+3V3 @ 2A
Q2
SM4307PSK
R192
10K
C201
2.2uF_10V_NL
R350
0
SLP_S3
{22}
{9,22,24}
VDDIO_SUS_PWRGD
{9,24}
SLP_S3#
U133A
SN74LVC1G08DBV
Q16
2N7002E
C199
0.1uF_10V
U17
APW8828
R188
2.2R
C195
10uF_6.3V
R216
200K
R187
200K_NL
OPTION FOR PFM/PWM MODE.
Fsw = 340kHz
C192
0.1uF_50V
R362
0
Q1
SM7304ESKP/KPAK
C187
10uF_25V
L4
2.2uH_7A_16.5mR
C355
0.0047uF_50V
C171
470uF_16V
C190
100UF_NL
C186
22uF_6.3V
C194
0.1uF_10V
R363
2.2R
+3.35V_ALW
4A@3V3 OCP 6A
3V3_PWRGD
{25}
R185
200K
RTOP
R189
3.3K_1%
R190
3.3K_1%
RBOT
R186
1.69K_1%
Vout = 0.68V * (1 + RTOP/RBOT) = +3.33V
R217
20K
C346
1uF_6.3V
RISE TIME TO 1.8V APPROX. 20MS. TBA.
C206
1uF_6.3V
U2
APL5915KAI
VIN#9
VIN#5
VCNTL
POK
EN
VOUT2
VOUT1
FB
GND
C205
22uF_6.3V
R204
20K
C351
1uF_6.3V
{25}
+1.5V_ALW_PWRGD
{23,25}
+1.8V_ALW_PWRGD
0.5A@+1.5V
+1.5V_FB
R220
27.0K_1%
C217
56pF_50V
R2
R221
30.0K_1%
R1
+1.5V_ALW
C212
100uF_6.3V
VOUT=0.8*(1+R2/R1) = 1.5200V
RISE TIME TO 1.8V APPROX. 20MS. TBA.
R338
20K
C350
1uF_6.3V
RISE TIME TO 1.8V APPROX. 20MS. TBA.
C193
100UF_NL
C191
100UF_NL
APU_VDDIO_SUS
APU_VDD_RUN
APU_VDDNB_RUN
+5V
APU_VTT_SUS
+1.8V
+0.95V
+3.3V
+5V_ALW
R136
4.7K
R237
4.7K
R231
4.7K
R141
4.7K
R323
4.7K
R95
4.7K
R263
4.7K
R346
4.7K_NL
R347
4.7K_NL
2mW DURING S0
+0.95V/+1.8V/+1.5V_ALW Power
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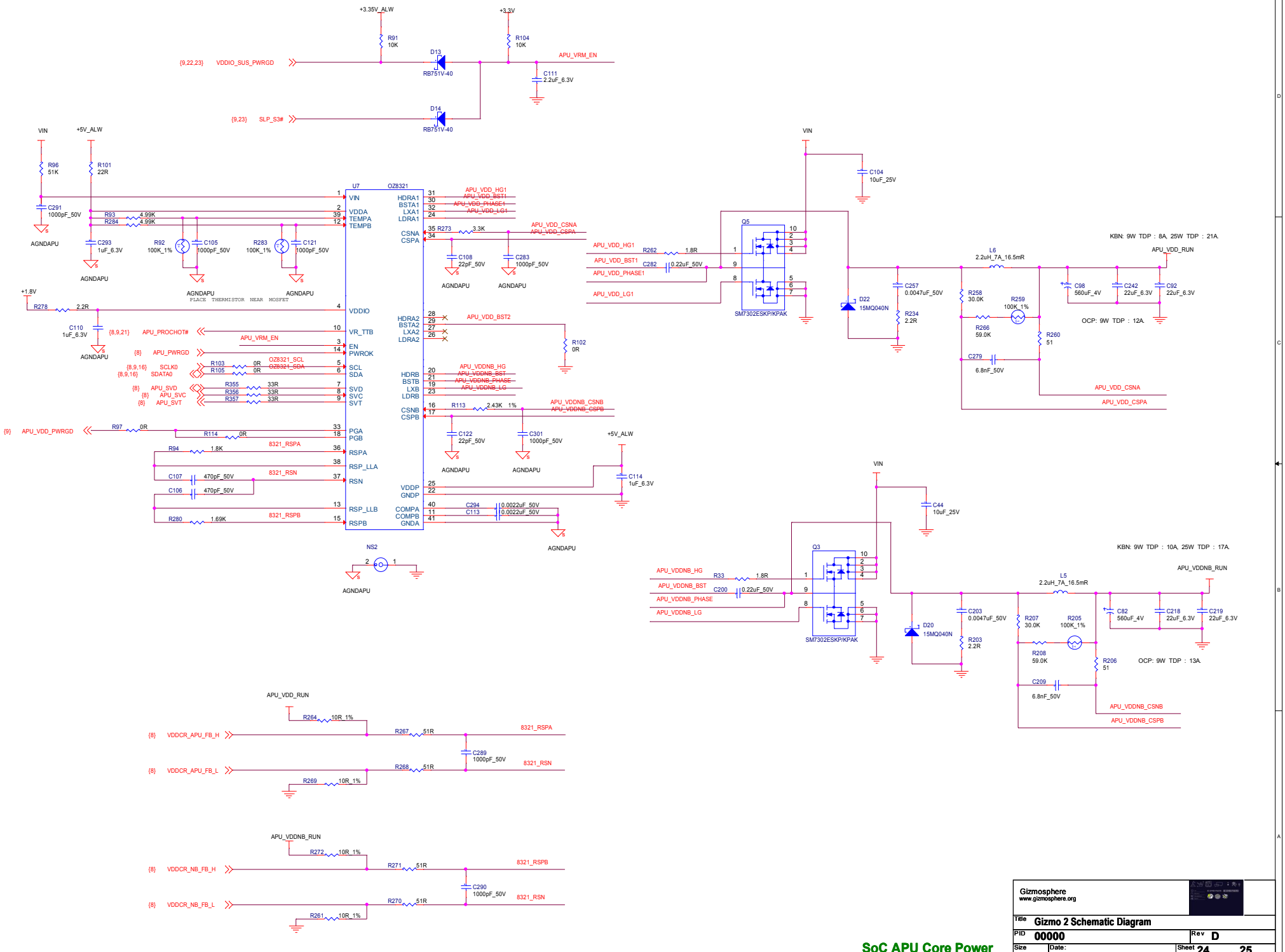

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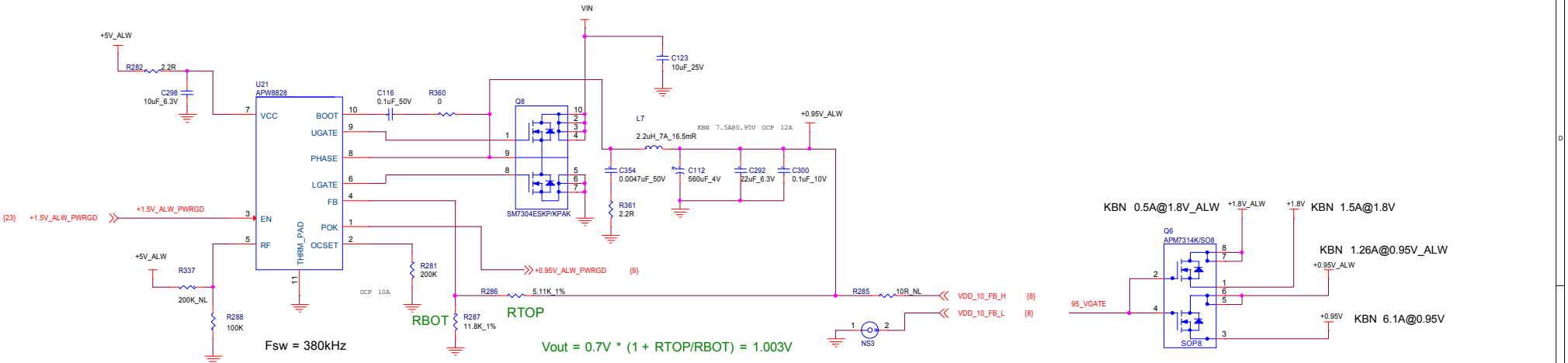
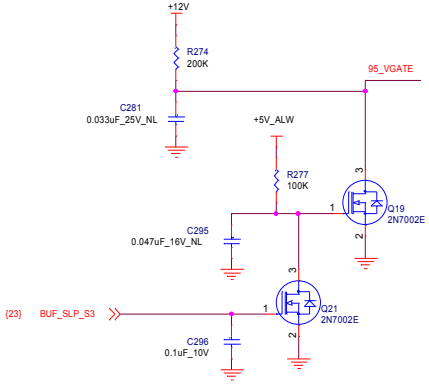
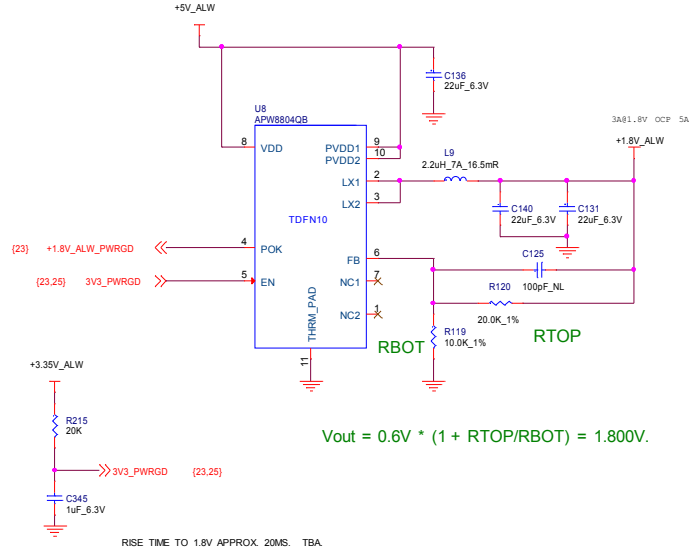
SoC APU Core Power





ACPI Control Table

	S0	S3	S5
SLP_S3#	1	0	0
SLP_S5#	1	1	0



+0.95V_ALW/1.8V_ALW Power

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