

REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	<ol style="list-style-type: none"> 1. Deleted R29-R44 from the LCD lines. 2. Added 47pf capacitors C156-C173 to LCD data lines to ground. 3. Changed schematic revision to A5A. 4. Changed a few footprints after PCB update for above changes. 5. Added access point for the battery function of the TPS65217C. 6. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. 7. Added power button to enable sleep, wakeup, power down and power up features on the system. 8. Added Modification to add 100K ohm resistor to ground to prevent crosstalk when serial cable is not plugged in. 	4/1/2013	GC

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

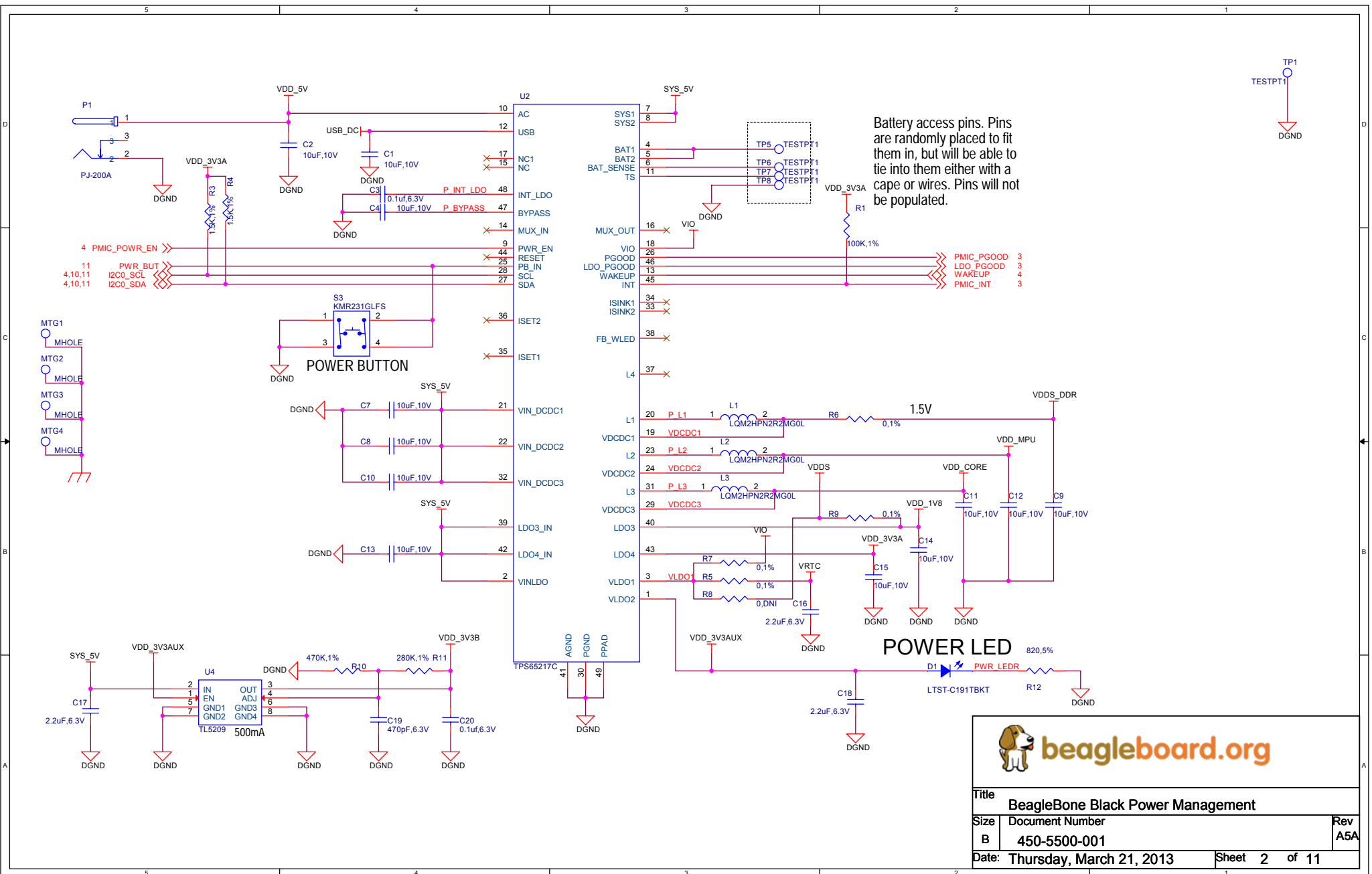
NOTE: PCB Revision for this board is Rev B3.

This schematic is ***NOT SUPPORTED*** and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.

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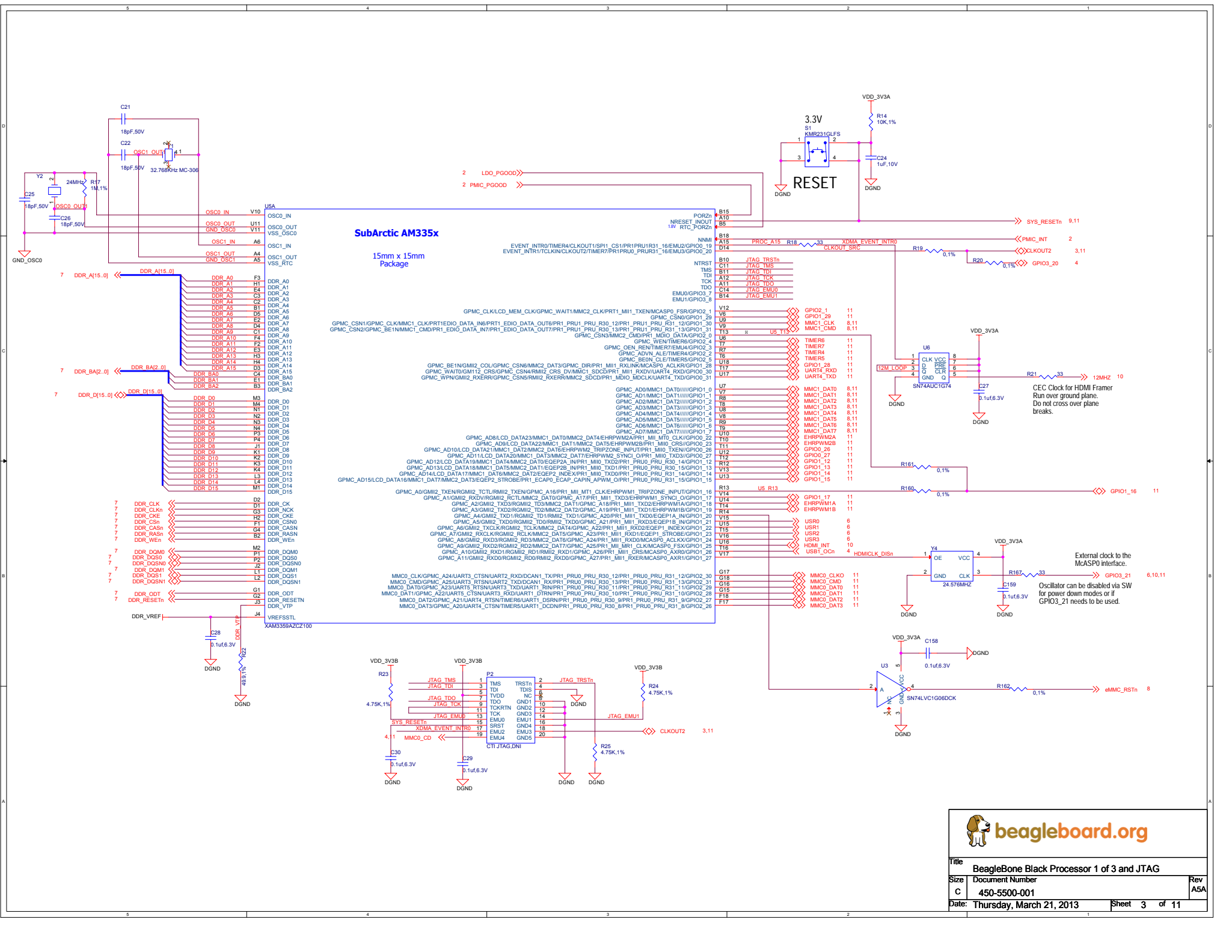

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Title		
BeagleBone Black Cover Page		
Size	Document Number	Rev
B	450-5500-001	A5A
Date:	Monday, April 01, 2013	Sheet 1 of 11




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Title		BeagleBone Black Power Management	
Size	Document Number	Rev	
B	450-5500-001	A5A	
Date:	Thursday, March 21, 2013	Sheet	2 of 11

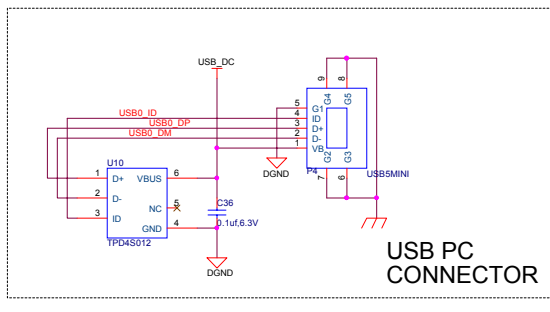
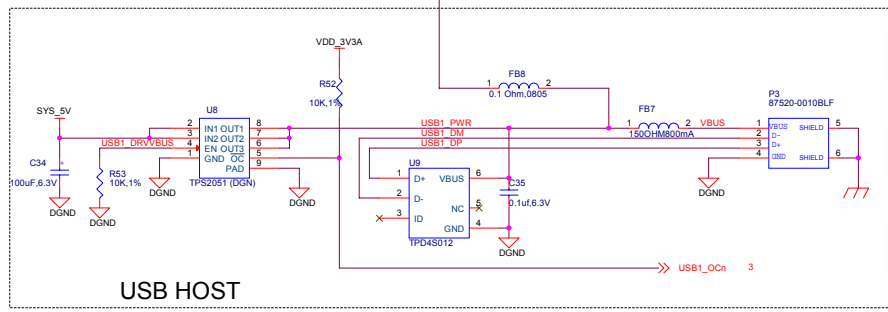


SubArctic AM335x

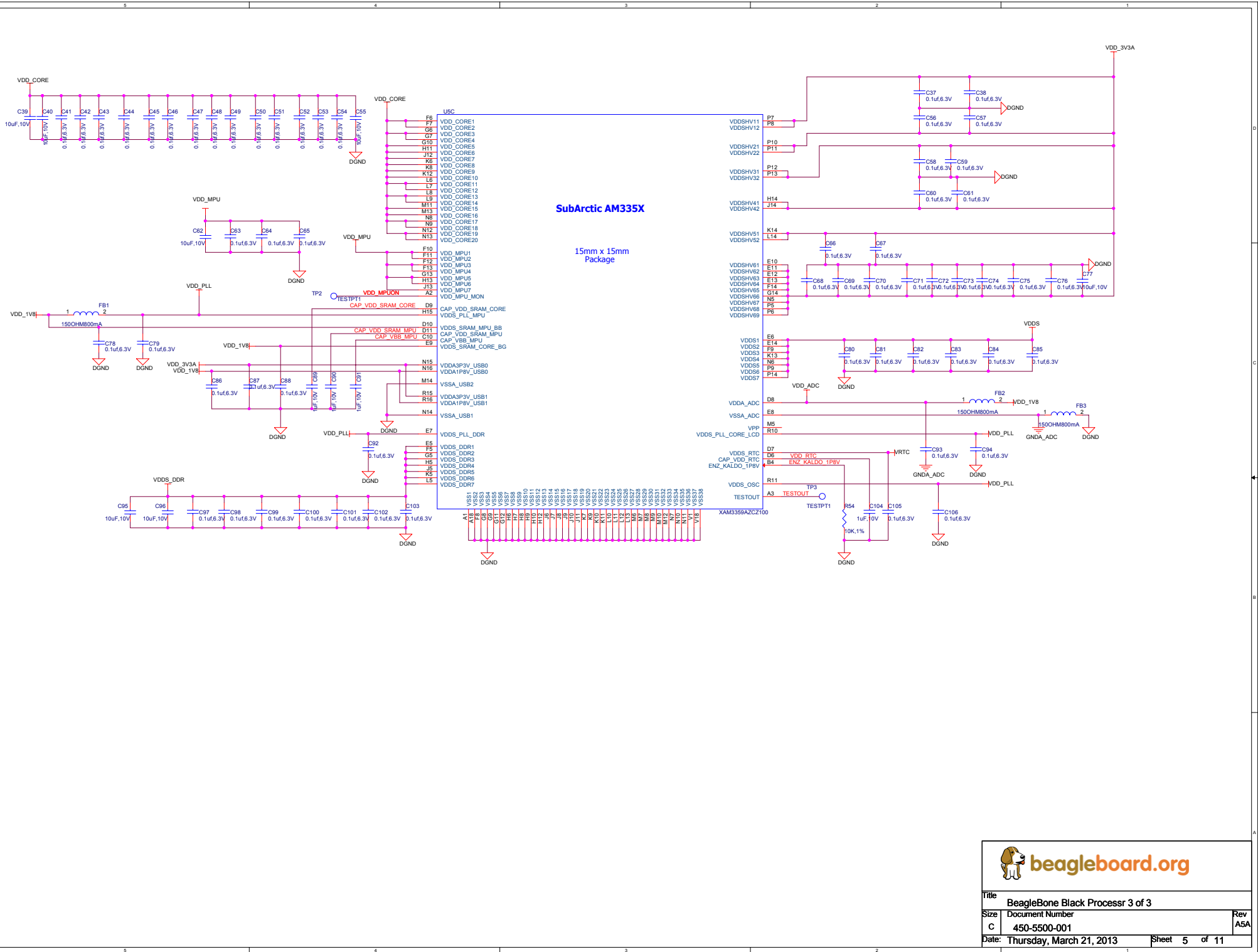
15mm x 15mm Package

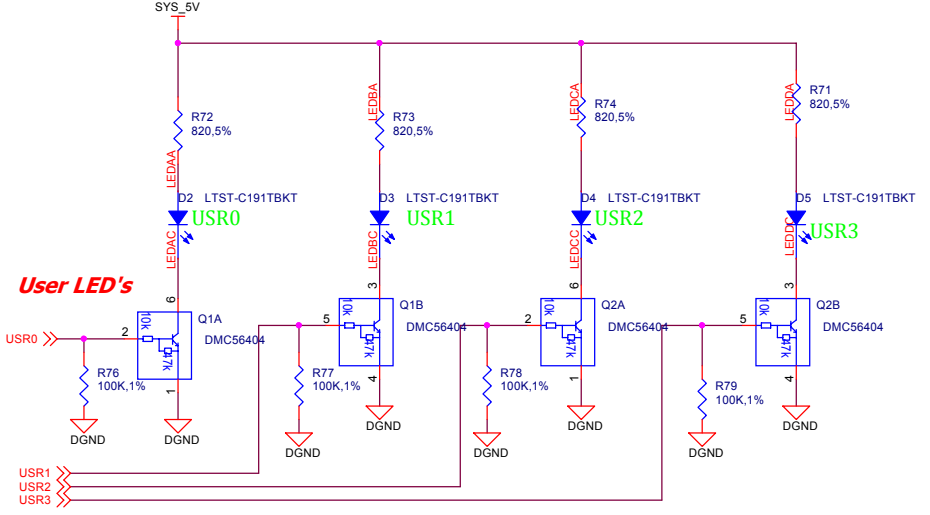
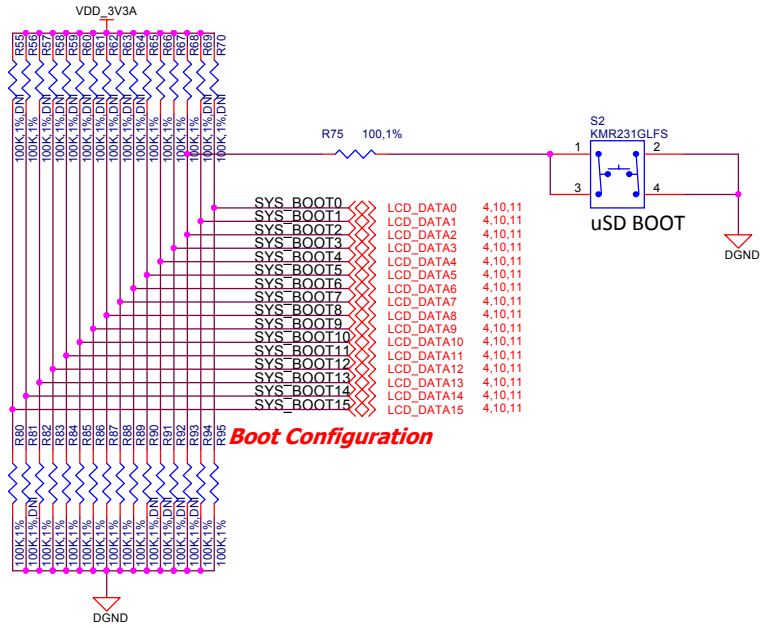


Title	BeagleBone Black Processor 1 of 3 and JTAG	
Size	Document Number	Rev
C	450-5500-001	ASA
Date:	Thursday, March 21, 2013	Sheet 3 of 11



Pin	Signal	Value
K17	MII1_TXCLK	9
K18	MII1_TXD0	9
K19	MII1_TXD1	9
K16	MII1_TXD2	9
K15	MII1_TXD3	9
J16	MII1_TXEN	9
H17	MII1_CRS_DV	9
H18	MII1_CRS_DV	9
H17	MII1_COL	9
L18	MII1_RXCLK	9
L16	MII1_RXD0	9
L15	MII1_RXD1	9
L17	MII1_RXD2	9
L16	MII1_RXD3	9
J16	MII1_RXERR	9
J17	MII1_RXDV	9
H18	MII1_REFCLK	9
M17	MDIO_CLK	9
M17	MDIO_DATA	9
R1	LCD_DATA0	6.10.11
R2	LCD_DATA1	6.10.11
R3	LCD_DATA2	6.10.11
R4	LCD_DATA3	6.10.11
T1	LCD_DATA4	6.10.11
Y2	LCD_DATA5	6.10.11
Y3	LCD_DATA6	6.10.11
T4	LCD_DATA7	6.10.11
U1	LCD_DATA8	6.10.11
U2	LCD_DATA9	6.10.11
U3	LCD_DATA10	6.10.11
U4	LCD_DATA11	6.10.11
V2	LCD_DATA12	6.10.11
V3	LCD_DATA13	6.10.11
V4	LCD_DATA14	6.10.11
T5	LCD_DATA15	6.10.11
V5	LCD_PCLK	10.11
U5	LCD_VSYNC	10.11
R5	LCD_HSYNC	10.11
R6	LCD_DE	10.11
A14	GPIO3_21	11
A13	SPI1_SCLK	10.11
B13	SPI1_DO	10.11
D12	SPI1_D1	11
B12	SPI1_CSD0	10.11
C13	GPIO3_19	11
D13	GPIO3_20	3

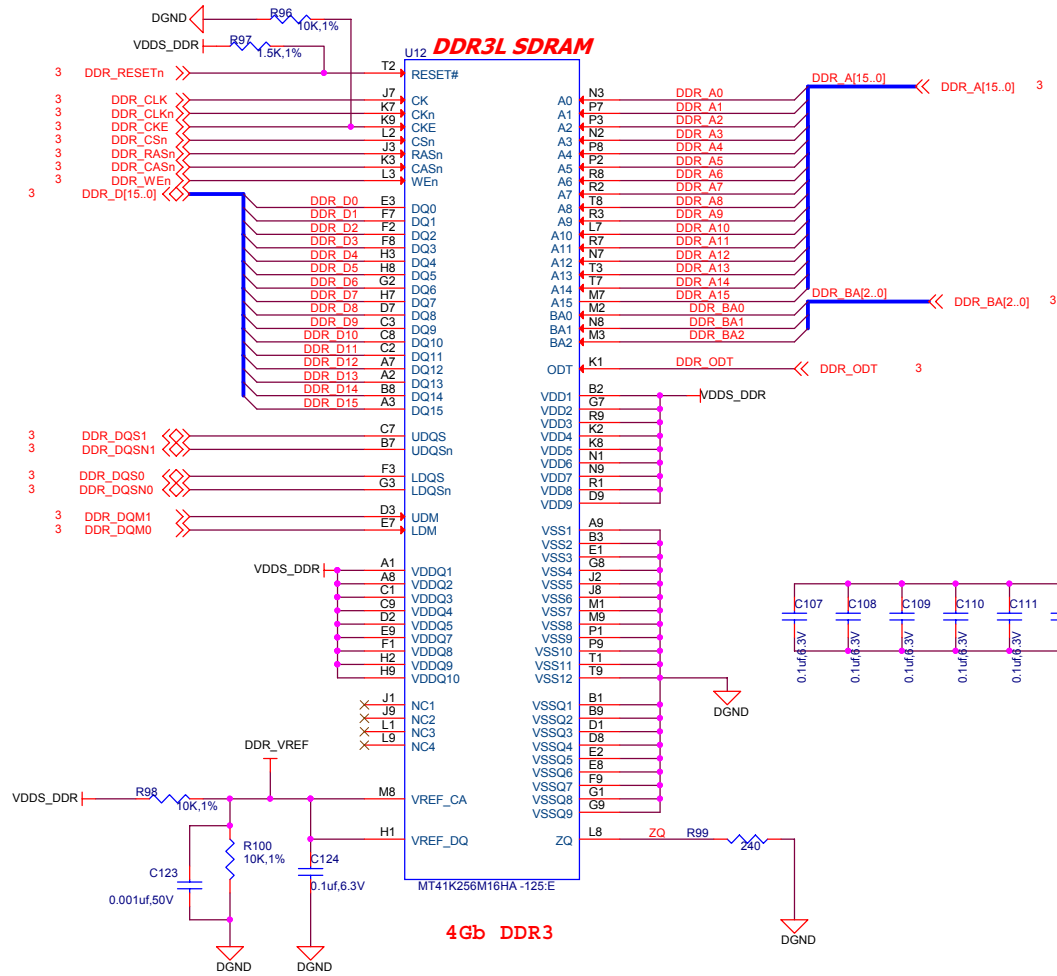




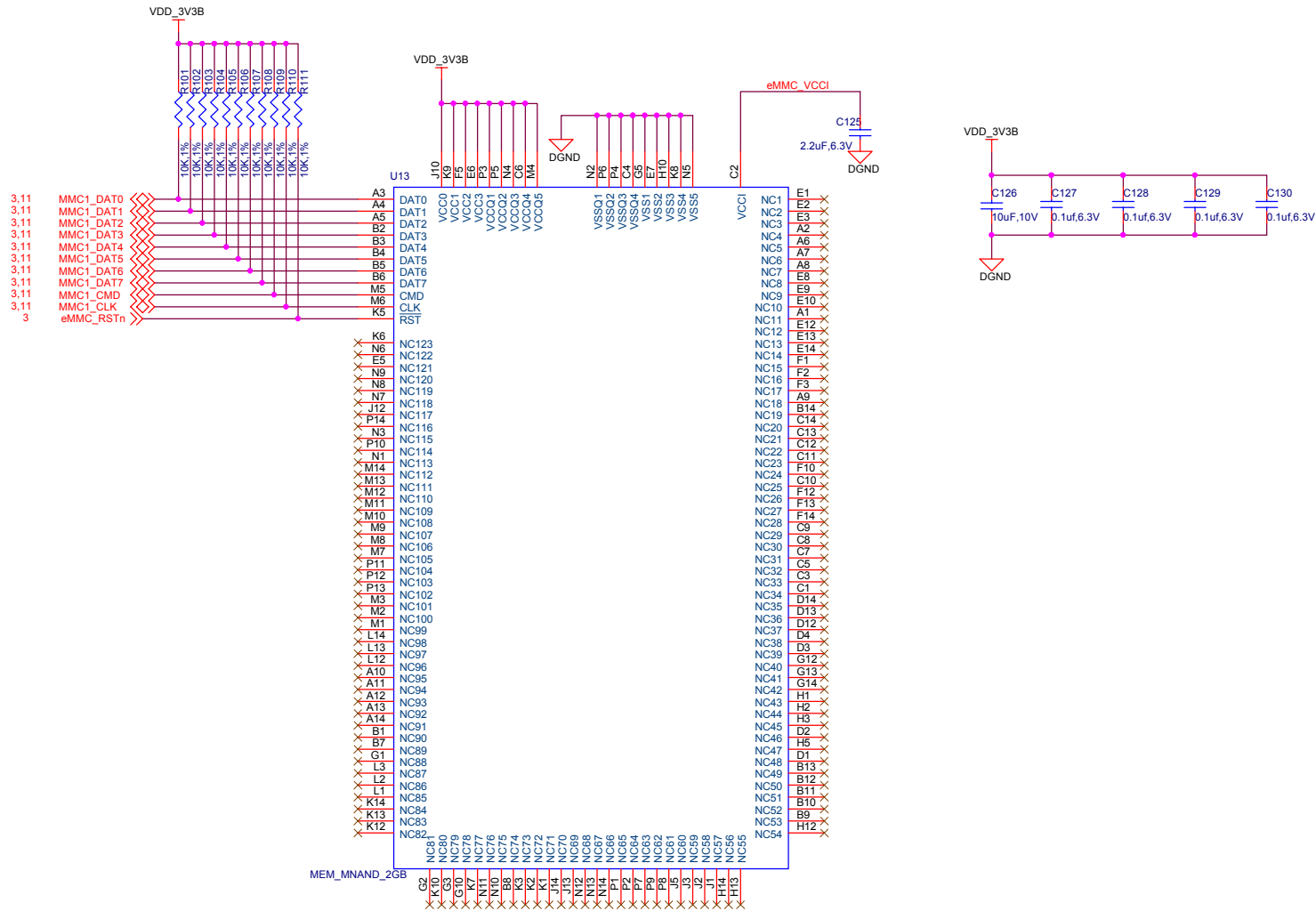
SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5] 1	UART0



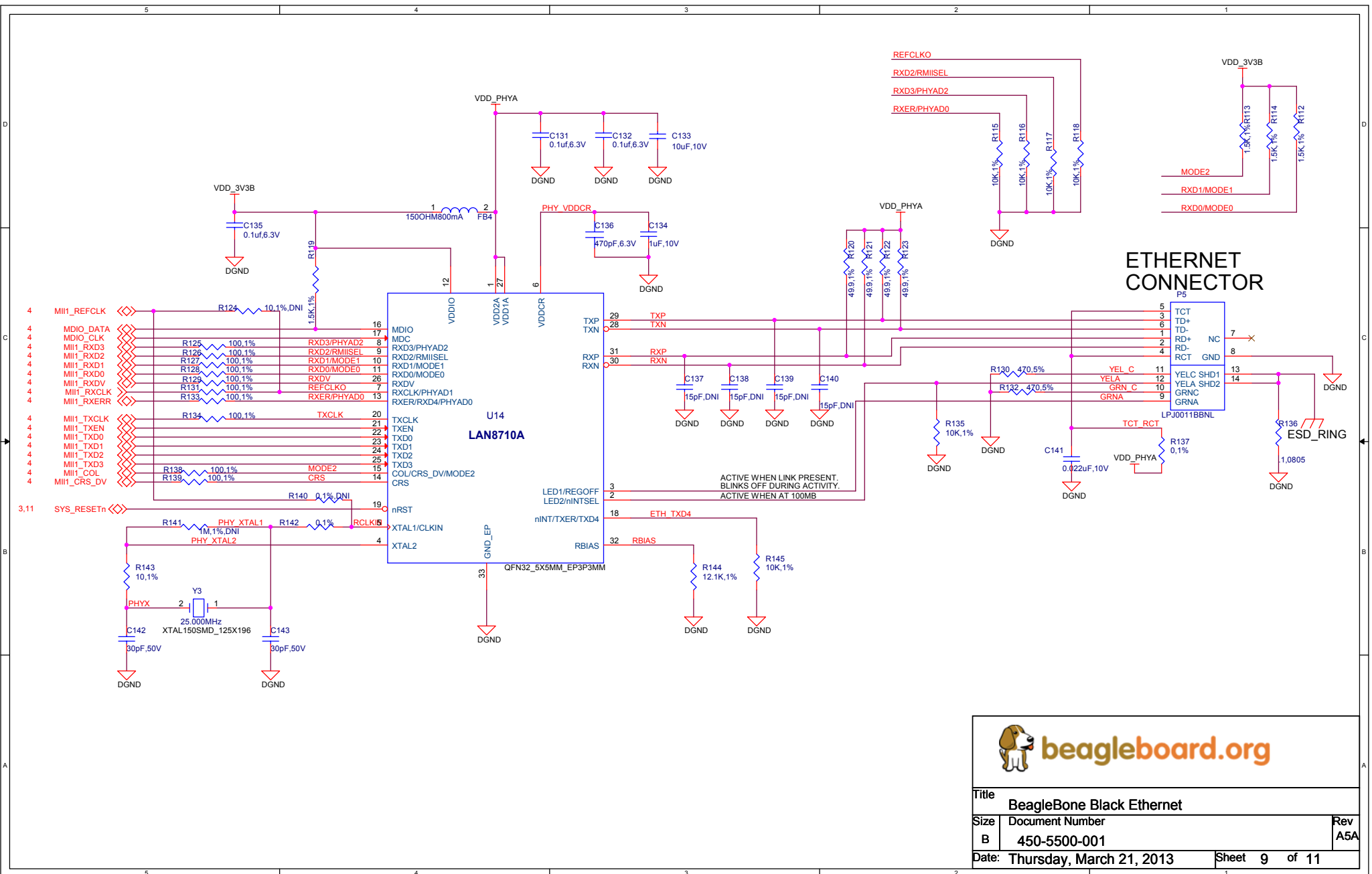
Title		BeagleBone Black LED, Configuration, and Reset	
Size	Document Number	Rev	
B	450-5500-001	A5A	
Date:	Thursday, March 21, 2013	Sheet	6 of 11



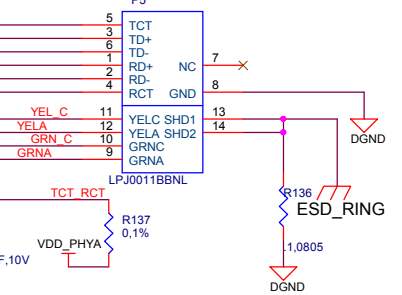
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BeagleBone Black DDR3 Memory		
Size	Document Number	Rev
B	450-5500-001	A5A
Date:	Thursday, March 21, 2013	Sheet 7 of 11



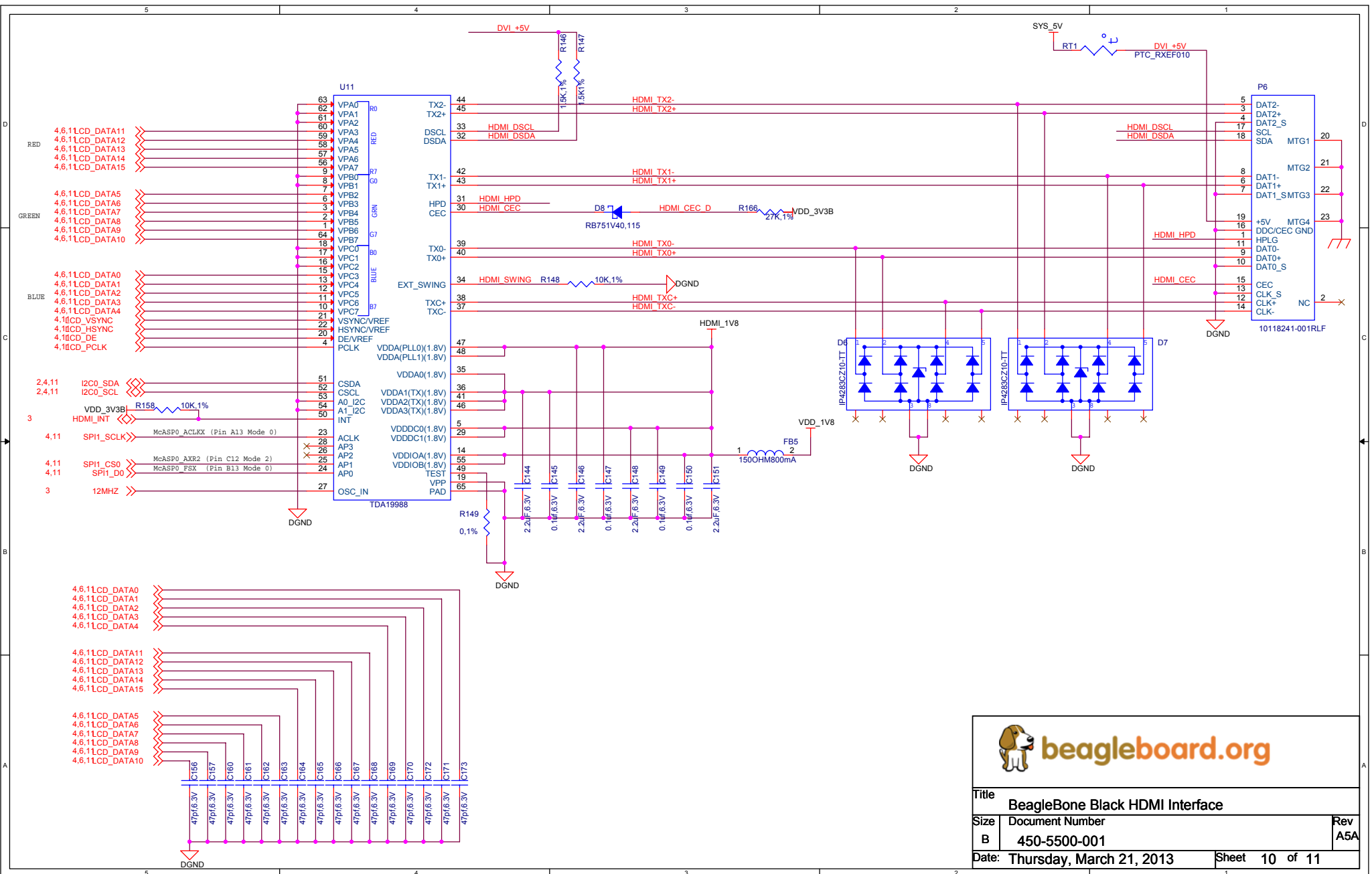

Title		
Beagle BoneBlack 2G eMMC		
Size	Document Number	Rev
B	450-5500-001	A5A
Date:	Tuesday, February 12, 2013	Sheet 8 of 11



ETHERNET CONNECTOR



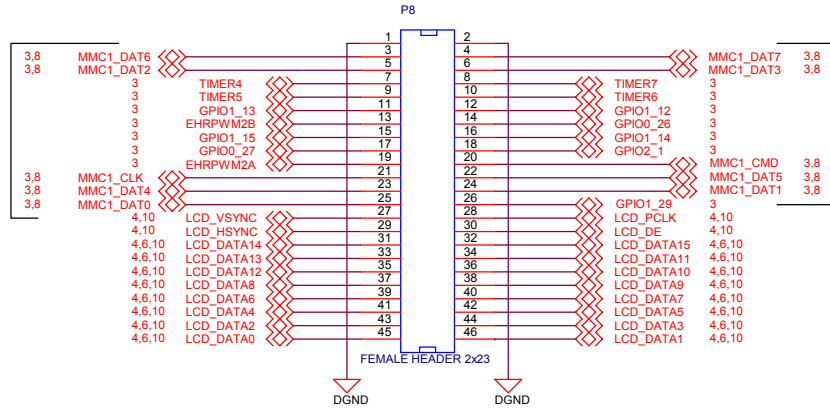
Title		BeagleBone Black Ethernet	
Size	Document Number	Rev	
B	450-5500-001	A5A	
Date:	Thursday, March 21, 2013	Sheet	9 of 11

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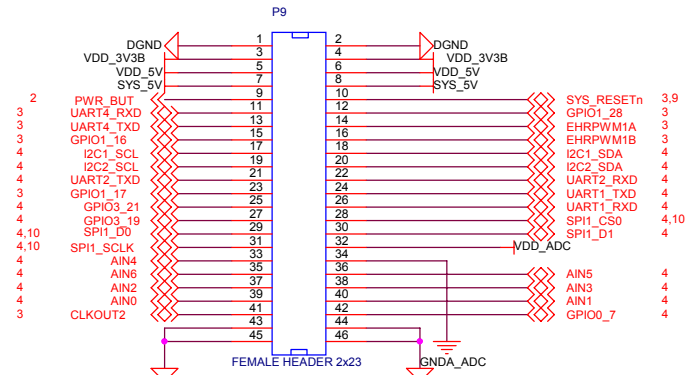
Title		BeagleBone Black HDMI Interface	
Size	Document Number	Rev	
B	450-5500-001	A5A	
Date:	Thursday, March 21, 2013	Sheet	10 of 11

CAUTION: USED ON BOARD

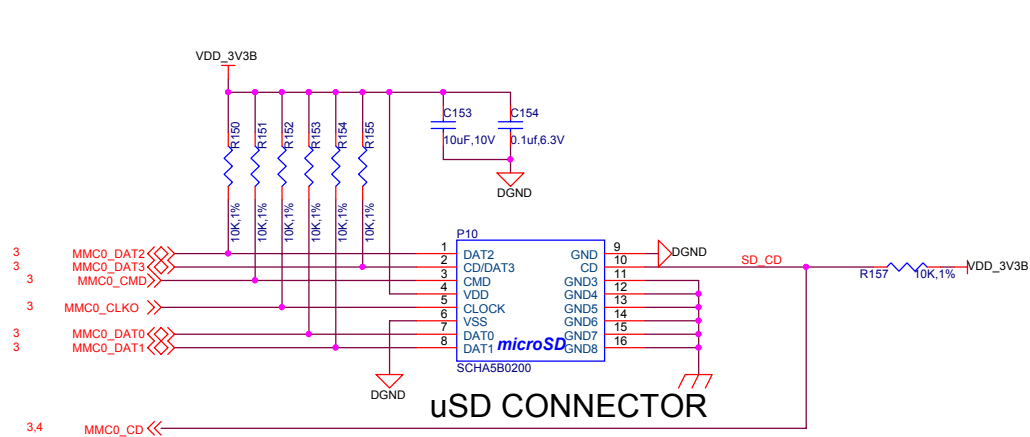


EXPANSION HEADER

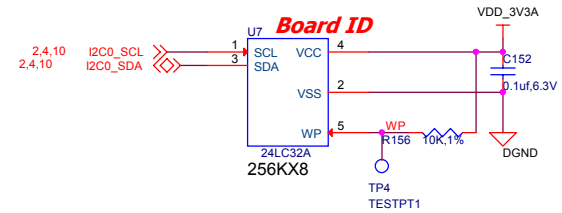
CAUTION: USED ON BOARD



EXPANSION HEADER



uSD CONNECTOR



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Title		
BeagleBone Black Expansion Headers, uSD and EEPROM		
Size	Document Number	Rev
B	450-5500-001	A5A
Date:	Monday, April 01, 2013	Sheet 11 of 11